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Simulation of power consumption in Low-Dropout Voltage Regulators in 90 nm technology

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Abstract: *A regulator design model is studied and simulated by using a dynamic bias technique. A dynamic bias boosting circuit consists of three parts: detector, amplifier and bias boosting circuit. The above Regulator is presented using CMOS 90 nm process and the obtained results will be examined with other existing technologies. The function of the diagram will be considered in this way that as soon as the slightest change is seen in output voltage; these changes will be transferred to the detector circuit through nodes Vn and Vp. The detector circuit makes sense of these changes and according to the type of detection, holds its output in the supply voltage situation or ground situation and will transfer it to the input of amplifier circuit. The amplifier circuit will work as an inverter and the detector's output will be appeared reversely in its output. The output of amplifier circuit is transmitted to the input of bias boosting circuit. This circuit, by increasing current, results in an increase in the regulated current in a short moment and returns the changes of regulator output voltage to the normal mode. In the discussed regulator, we reduced the power consumption using dynamic bias current to .5 mw and to some extent improved the line and load-transient response. The Technique of increasing the dynamic bias current in LDO design effectively improves the linear and load transmission response and leads to the creation of a precise and affecting voltage in the regulator's output and will be very effective in portable applications where an accurate and noiseless power supply is require.*
Keywords: *Low-Dropout Voltage (LDO), regulator, dynamic bias, speed detector.*

INTRODUCTION

The management of circuit power in moving systems, such as radio frequency devices and medical instruments is considered to be very important so that the power supply in these systems are more limited. (Ho and M, 2010). In addition, a chip capacitor as a source of energy storage and stable output voltage is not available in these systems. As a result, a Low-Dropout Voltage regulator with a relatively simple structure will be considered for moving systems (Shen et al, 2013). In any case, the most important feature of low power LDO is having a rapid transition and an increased rate of speed but it is difficult to obtain it. Recently, dynamic bias is considered from effective ways to improve the transitional response in low power design (Chen chang, Wing, 2011). Interruption and dynamic bias are shown in Figure 1. Bias current improves the bandwidth and speed in the system. Increasing the bandwidth is required when there are rapid changes of load current or output voltage in the circuit. Increasing the dynamic bias current can be done in a short moment. A comparison with other methods of non-dynamic bias has been shown in Table 1. (Gangopadhy et al, 2014).

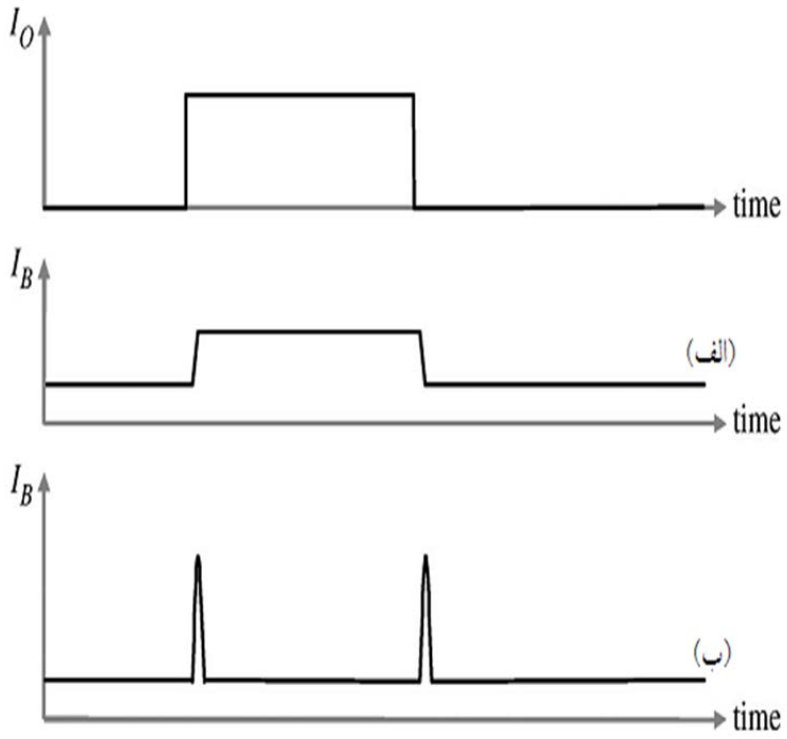

Figure 1: bias current in LDO regulator (A) interruption bias (b) dynamic bias

Table 1: Comparison of bias methods (dynamic and interruption)

year	2010	2010	2012	This work
Biasing method	Dynamic	Dynamic	Dynamic	Dynamic
Sleving Detection	Output	Internal	Internal	Internal
Improvement	Slew-rate and Bandwidth	Slew-rate Only	Slew-rate and Bandwidth	Slew-rate and Bandwidth
Automatic Shot-off	Yes	No	Yes	Yes

A dynamic bias-current boosting technique

The diagram of dynamic bias boosting circuit for LDO is shown in Figure 2. This circuit includes a speed detector, amplifier and bias boosting circuit. The diagram's function will be considered in a way that as soon as the slightest change is seen in the output voltage, these changes will be transferred to the detector circuit

through nodes Vn and Vp. The detector circuit makes sense of these changes and according to the type of detection, holds its output in the supply voltage or ground situation and will transfer it to the input of the amplifier circuit. The Amplifier circuit will work as an inverter and the detector's output will be appeared reversely in its output. The output of amplifier circuit is transmitted to the input of bias boosting circuit. This circuit, by increasing current, results in an increase in the regulated current in a short moment and returns the changes of regulator output voltage to the normal mode.

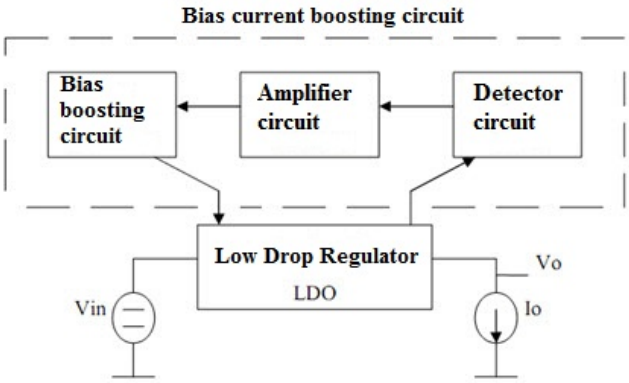

Figure 2: Diagram of dynamic bias-current boosting technique

Speed detector circuit

A current mirror amplifier is shown in Figure 3. In a detection period, input V $_{(IN+)}$ and V $_{(IN-)}$ are asymmetrical and cause many changes in the internal nodeV_N. Based on the detection mechanism, the complete improvement of speed detector circuit is shown in Figure 4. In fact the function of the speed detector circuit is in a way that connecting the circuit output to the ground or power supply is possible by changing the voltages of V_p andV_N. These voltages will be biased in steady state by the current mirror amplifier. V_{HI} Will be biased when the supply voltage is connected to it and V_{LO} will be biased when the ground is connected to it that the pair transistors is shown in Fig. 5 by the VI characteristic. Continuous lines especially show the relations between V_{DS} and I_{DS} for NMOS transistor in $(\frac{W}{L})_N$ and dotted lines differently show the relations between V_{SD} and I_{SD} for PMOS transistor in$(\frac{W}{L})_P$.

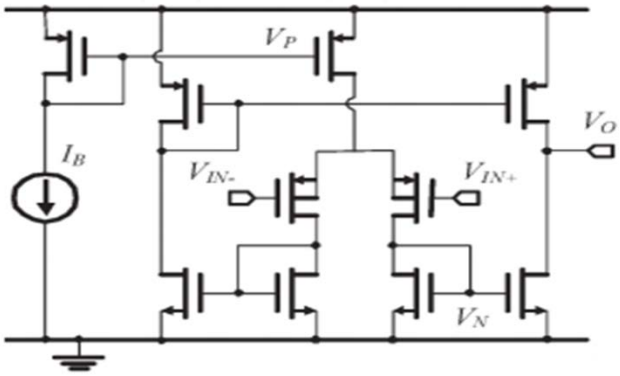

Figure 3: A typical current mirror amplifier

NMOS and PMOS transistors are placed in series and I_{DSN}=I_{SDP} and V_{SDP}-V_{DD}=V_{DSN} that V_{DD} can be considered a supply voltage. In a specific $(\frac{W}{L})_N$ and $(\frac{W}{L})_P$ the output voltage of (V_{HI} and V_{LO}) is biased in V_1 (about 0.5 V_{DD}) and the I_2 is the current in each transistor.

If the ratio of PMOS transistor to the level of $(\frac{W}{L})_P \frac{3}{2}$ be increased, the output voltage will reach V_3 and the drain current of I_3 will be identical in both transistors. If there is a reduction in the ratio of PMOS transistor to $0.67(\frac{W}{L})_P$ then the output voltage will drop to V_1 and the drain current of I_1 will be the same in both transistors. Therefore, V_{HI} and V_{LO} can alternatively be connected to the supply voltage and the ground.

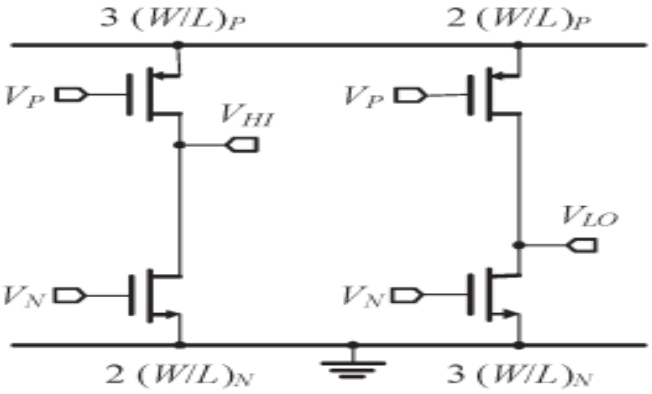

Figure 4: The speed detector circuit

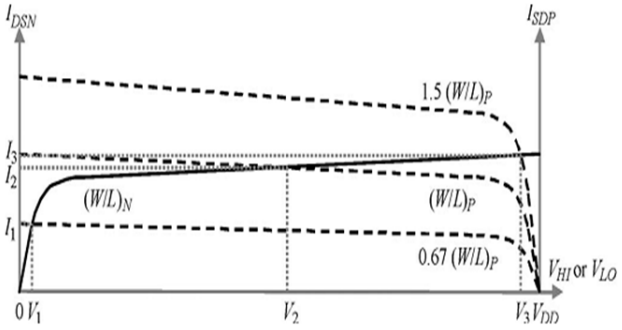

Figure 5: Voltage Specifications- the current of speed detector circuit with different dimensions of transistor

Amplifier circuit

A trigger signal is used to generate quick returns in the circuits of bias amplifiers. The amplifier circuit will be considered as CMOS with a simple structure. Waveform signal in the amplifier circuit is shown in Figure 6. (V_{HI} and V_{LO}) are connected to the input of an inverter and create the output of V_{UP} and V_{DOWN}. When the positive speed becomes apparent V_O slowly increases based on the level of speed. In this case, the V_p voltage is low and a large V_{SG} is created to provide the maximum current in the PMOS transistor. Similarly, if the

negative speed becomes apparent, V_N will increase and both (V_{HI} and V_{LO}) will be pulled down. (Liao, Samuel, 2000)

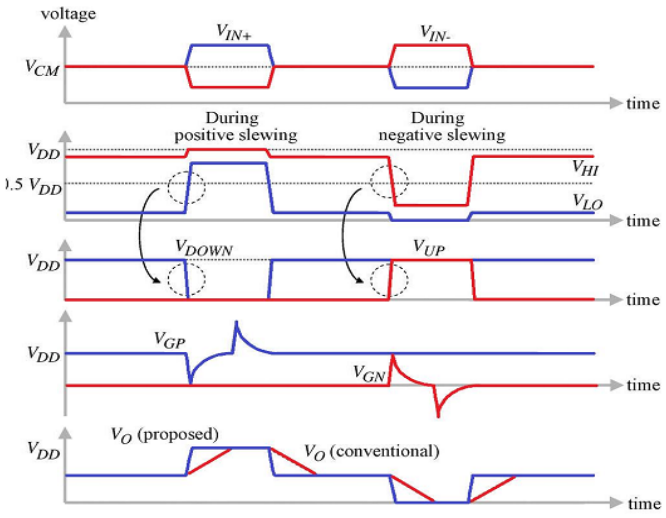

Figure 6: The signals of bias boosting circuit and amplifier during detection

Bias boosting circuit

A bias boosting circuit (Figure 7) provides a full signal increase in each two positive and negative periods. V_{UP} and V_{DOWN} are alternatively produced by speed detector circuits and amplifier circuits. At a steady state, the level of V_{UP} is low and the level of V_{DOWN} is high and both of the transistors, M_{BP} and M_{BN} are off. Bias current of I_B will be achieved by V_B and series resistances of R_{B1} and R_{B2} A high-pass network including C_N , R_N, C_P and R_P can turn on both transistors of M_{BP} and M_{BN}. The level of R_N will control the isolation between V_{GN} and the ground and C_N controls the ability of trigger signal coupling. R_N and C_N will be 1MΩ and 5PF respectively. In fact, these amounts are considered to produce pulse 1 µS with current amplitude of 20 µA to set up 6PF gate capacity when the supply voltage is 9V. Current will be established in the transistor in a short moment that the pulse arrives. As a result, V_X and I_B will increase. After the end of the pulse, M_{BP} and M_{BN} transistors are turned off automatically.

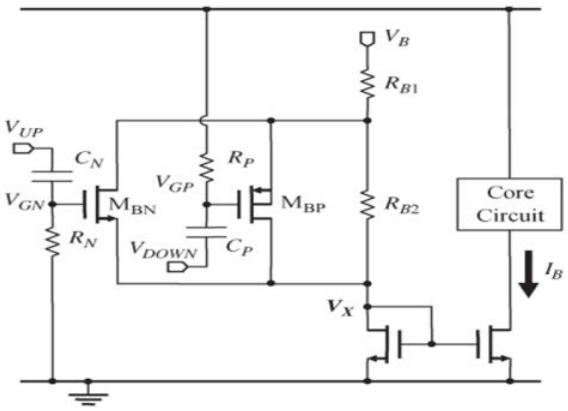

Figure 7: Bias boosting Circuit

Ultra-Low Power LDO by using Dynamic Bias-Current Technique

A dynamic bias current boost circuit is shown in Figure 8 for ultra-low power LDO using CMOS 90nm process. Design parameters are shown in Table 2. The designed I_B will be considered lower than 10nA and the idle current of LDO will be equal to 1.28 µA. Figure 9, shows the simulation results of LDO's frequency response in the normal bias (10nA =I_B) and also shows the maximum bias current (20µA = I_B) with the capacity of 10nF for the output capacitor. We will see that the LDO's frequency will be increased from 8.5 KHz to 217.9 KHz while the phase margin will reduce from 89.4 to 87 degrees. So we'll see that dynamic bias boosting technique, regardless of its stability, will improve the response time. When the bias increases, the error amplifier output pole P_{EA}, will be drawn to high frequencies. To illustrate the improved linear and load response through bias boosting technique, the discussed LDO is simulated along with the contractual LDO which is the same as discussed LDO without considering C_N ، R_N ، C_P and R_P. Both regulators of LDO have power 9V, Output 2V, and maximum load current of 50mA. The LDO's load responses are shown in Figure 10. Both of them have load changes from 0 to 50mA in 200nS. It should be noted that I_B, discussed LDO will be considered immediately and temporary in each two positive and negative periods. Therefore, the response time of the discussed LDO is considered much faster than normal LDOs. Dynamic bias technique is very effective in increasing the linear response when we use low power consumption LDO.

Table 2: Parameters of the proposed LDO

Transistors	Size (µm/µm)
M_{01}–M_{03}	20/1
M_{04}–M_{09}, M_{B1}–M_{B3},	10/1
M_{BN}, M_{BP}, M_{A1}–M_{A4}	10/0.18
M_{SD1}, M_{SD4}	20/1
M_{SD2}, M_{SD3}	30/1
M_{PT}	6000/0.18
Resistors and capacitors	**Value**
R_N, R_P	1 MΩ
C_N, C_P	5 pF
R_{FB1}	82.5 kΩ
R_{FB2}	577.5 kΩ
R_{B1}	20.6 kΩ
R_{B2}	3.7 GΩ

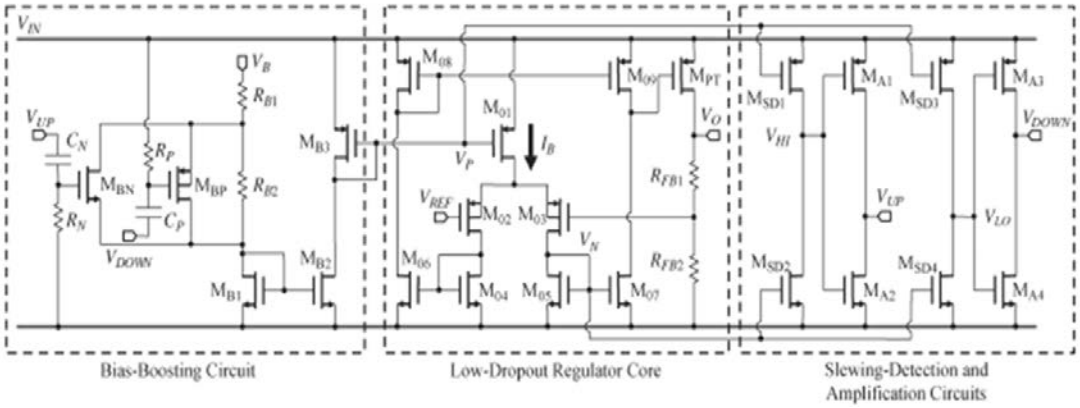

Figure 8: LDO circuit by using the dynamic bias current boosting circuit

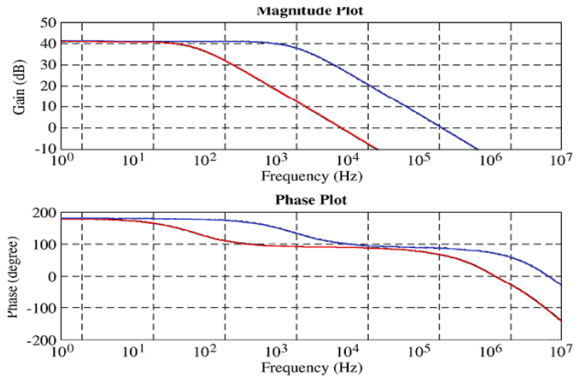

Figure 9: the simulation of frequency response with 10 Nano vamps bias current (red) and 20 micro amps (blue)

The simulation result

An LDO is considered through the dynamic bias current boosting circuit by using CMOS 90nm process. In addition, a contractual LDO without the proposed circuit was used for comparison. Resistor and capacitor values are respectively considered 1MΩ and 5PF for simulation. Both LDOs have the output capacity of 10nF in the stable mode and can provide 50mA output current with 2V voltage while the power supply is 9V. The LDO's discussed and contractual idle current will be 1.25 mA and 1.28 mA respectively, figures 10 and 11 show the line and load response for both LDOs. The load current changes from 0 to 50mA within 200nS and with V_{IN}=0.9. The contractual LDO needs time of about 300nS for these changes while the discussed LDO consumes time approximately 9nS to 28nS for increasing or decreasing the load. Bias current will increase about 10nA, to a high of 20µA. For positive and negative changes of the input power, the discussed LDO needs time between 36µs to140µs while the contractual LDO, with the same changes, needs time between 118µs to 220µs.

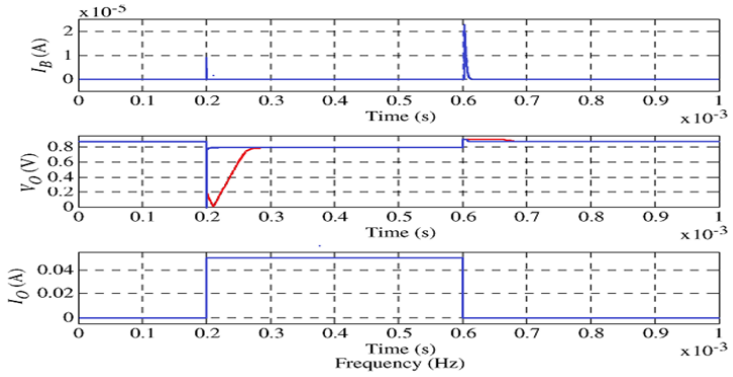

Figure 10: Simulation of the load transient response in a normal regulator (red) and discussed regulator (blue)

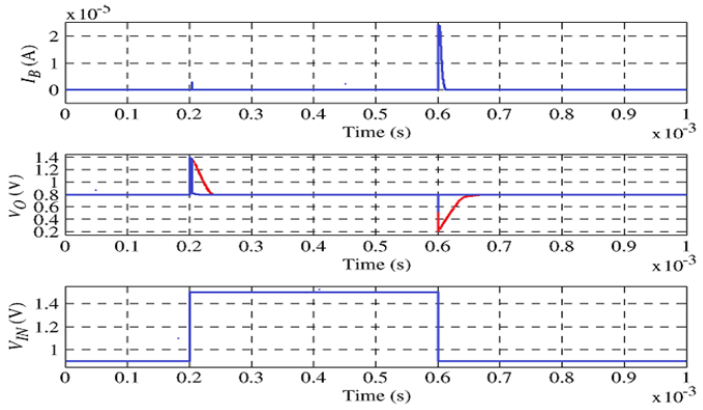

Figure 11: Simulation of the line transient response in a normal regulator (red) and discussed regulator (blue)

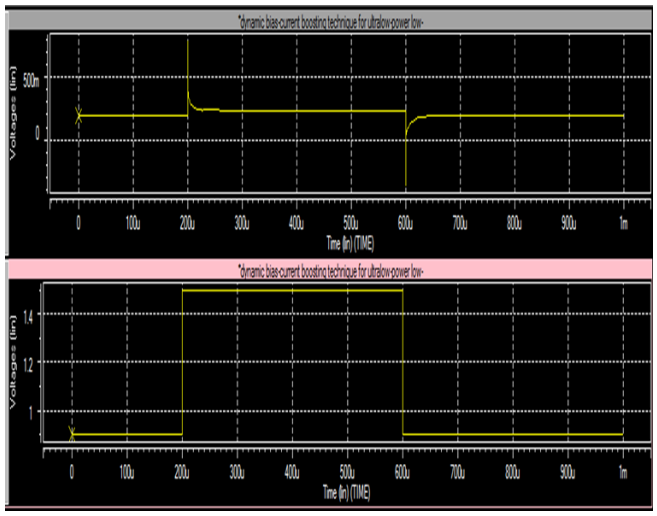

Figure 12: The simulation of the line transient response in discussed regulator

Discussion and conclusion

In this article, the regulator has the input voltage of 9 volts, output capacitor 100 Pico farad and output current of 50 mA at 90 nm technologies in which the output voltage is 2V and the DRAPOUT voltage is 0.1 V and gives us 40dB. In the discussed regulator we reduced the power consumption to a low of 0.5 mw by using dynamic bias current and to some extent improved the line and load transient response. The dynamic bias boosting current technique in the design of LDO will effectively improve the line and load transmission response and makes a precise and effective voltage in the output of the regulator and is very effective in portable applications which require an accurate and noiseless power supply. Designing the regulator based on the method of dynamic bias current reduces the circuit current and thus the drawn current from the battery is reduced and can increase battery life. Reducing the DRAPOUT voltage cause reduction in power dissipation, increase efficiency and consequently, improves the load charging. As was observed, the quiescent current, (Iq) and Vdo partially reduced which results in longer battery life and an increase in the speed of response. Designing the regulator based on dynamic bias current reduces the circuit current and thus the drawn current from the battery is reduced and battery life will increase. Table 3 compares the discussed regulator with other works.

Table 3: Comparison of discussed regulators with other works

	[9]	[10]	[11]	
Year	2010	2010	2012	This work
Biasing Method	Dynamic	Dynamic	Dynamic	Dynamic
VoutΔ [mV]	144	90.3	880	600
I_Q	19µ	20µ	1.33µ	1.28 µ
Automatic shut-off	Yes	No	Yes	Yes
Gain[db]	58	55	46	40
V_{OUT}	0.8 V	1.6 V	0.8 V	.2v
V_{DO}	0.2 V	0.2 V	0.1V	.01v
I_{OUT}	66.7mA	100mA	50mA	50mA
Tech[µm]	AMS CMOS .35µm	AMS CMOS .35µm	CMOS .18µm	CMOS 90nm
C_{OUT}	100PF	100PF	100PF	100PF
Current efficiency**	99.972%	99.98%	99.997%	99.9974%

To improve and increase the speed of the circuit, an analog bootstrap can be use between error amplifier and power transistor in the LDO's structure. Frequency compensation can be utilized in LDO's structure to improve and increase the stability of the circuit. Different structures can be used to by-pass power for more integration and less input power. Also by drawing the circuit's Layout, the chip area occupied can be calculated and compared with other works.

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