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Investigating 4: 2 Compressors in Different Threshold Voltages

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Abstract: *In recent years, digital multiplication circuits are used extensively in microprocessors, signal processing, encoding algorithms as well as computing the efficacy of algorithms. 4 to 2 compressors are generally used for plus operations. The purpose of this study is to investigate these compressors and conducted researches in relation to the way of working and structures of 4 to 2 compressors. The methodology of this study is descriptive-analytical and data was gathered using different studies inside the country and out of country. Data collection instrument include articles, internet sources and written documents in this field that are collected by using fishing technique. The results of this study indicate that the main characteristics of 4 to 2 compressors are compression level of 2 and using as the base cell to male bigger compressors including 6 to 2, 9 to 2 and finally IEEE 754standard (compressor 27-2). But it seems that the result of researches conducted by engineers show that 4 -2 compressor is not able to multiply and plus of consecutive numbers. In Keyvan, a new technique is presented to plus numbers in which a circuit is designed by using multi-circuit logic that at the same time has all characteristics. In new design, in addition to simplicity of plus numbers, the delay for the best and worst path is exactly the same.*

Keywords: *4-2 Compressor, Voltage, Multiplier.*

INTRODUCTION

In recent years, many researches are done in the carbonnanotube technology.1–6 Since integrated circuits in MetalOxide Semiconductor Field Effect Transistors (MOSFET)technology keep to scale down into nanometer limitedareas, this art is starting to face various troublous challenges.Several of these challenges are: intensive processvariations, decreased gate control, increased short-channeleffects, and exponentially rising leakage currents.3 As aresult, new devices are required to alternate MOSFETtechnology and eliminate these problems. The CarbonNanotube Field Effect Transistor (CNFET) is one of thepromising new devices. Because of their specific electronicand mechanical features, CNFET is a considerable field ofNano electronics. One of the most considerable characteristicsof this kind of transistor is ability of having optionalthreshold voltage by changing the diameters of the nanotubes.This feature makes CNFETs proper for designingcircuits with multiple threshold voltage ranges.5_ 7In many VLSI systems, low power and fast arithmeticunits such as adders and multipliers are the most vastlyand regularly used circuit. These modules are most criticalblocks of arithmetic constructions. So efficiency of thesemodules will largely influence the total circuit efficiencyin term of speed and power consumption.8_ 9Multiplication is one of the fundamental arithmetic operationsin digital

signal processors and microprocessors.∗Author to whom correspondence should be addressed.Microprocessors use multipliers within their arithmeticlogic units; digital signal processing systems need multipliersto implement DSP algorithms such as filtering andconvolution.6 Thus, enhancing the efficiency and speed ofa multiplier is beneficial. A multiplication process includesof three phases: Partial products generation, partial productsadditions and final addition. The partial products additionis the most serious phase and defines delay, power andarea of the multiplier. Thus for acquire partial products,compressor cells usually perform this stage because theycontribute to the reduction of the partial products and alsocontribute to decrease the critical path which is serious tomaintain the circuit's efficiency.10_ 11In this paper, a high speed 4-to-2 compressor cell isproposed for fast digital arithmetic integrated circuits. The4-to-2 compressor has been widely employed for multiplierrealizations. CNFETs with different threshold voltageare used to design proposed 4-to-2 compressor. Proposedstructure is optimized and simulated in different supplyvoltage and it is compared with other state-of-art structures.Simulation results show great achievement in timedelay. The performance of our proposed 4-to-2 compressorhas been thoroughly checked under different temperatures,frequencies and load capacitors.

Multiplication is the most important arithmetic operation in many applications executed on common and specific purpose digital processors. A multiplication process consists of three phases: partial product generation, partial product reduction, and the final carry propagating addition. The most area consuming and power dissipating part among aforementioned three phases is partial products reduction. This phase has received a lot of attention by researchers of digital multipliers (Reshadinezhad et al., 2012; Asgari & Sachdev, 2004).

In multiplication hardware and multi-operand addition, compressor cells seem to be the most generic bit-compressing cells with main application. Digital multiplication circuits are used extensively in digital signal processors and microprocessors. Performance of many arithmetic algorithms depends on multiplier's efficiency (Navi, et al., 2008). Due to the critical role of compressor cells in the design of efficient multipliers, the comprehensive study of design alternatives of these cells was motivated. Compressor cells are used in multiplier circuits in order to reduce the number of partial products. The advantages and performance of compressor cells are understood via gate level analysis.

Theoretical framework

Common 4:2 compressor

Implication of 4-2 compressor shows that critical path in these compressors include three xor gates placed in the output s path. But 4-2 compressor has other designs. Interesting point is that there are separate circuits for co output and describing s output based on x1+ x2 +x3. 4-2 compressor is connected like a chain by using partial output/input.

In this case c0 output from compressor in lower levels is connected to ci input in the higher levels.it should be noted that because of not mentioning digits co output should be a function of ci

$S=p \oplus ci$ (1)

$C = x4\bar{p} + cip$(2)

$C0=(x1 \odot x2)x1 + (x1 \oplus x2)x3$ (3)

$P=x1 \oplus x2 \oplus x3$ (4)

Compressor is the most important unit in electronic circuits. In general, it's an adder for multioperations. Processor plays the main role in a processor circuit. So, an effective compressor can cause a high speed processor with lower power. This unit is used in multiply tree reduction and adding multi operations.

Diameter and Kiara lite vector of CNFET transistors

As it's mentioned before, carbon nanotubes are monolayer or multilayer ovals that are conductor or semi conductor based on carbon atom arrangement. In other words, type and angle of carbon atom arrangement in gryphon and in general in nanotubes are based on Kairalitevector and integral numbers of n1,n2. This vector is shown with $C_h$and is computed according to equation (1-1). Pair vectors are determined based on the relationship between n1, n2. It means that if n1, n2 are the same and nonzero, armchair vector (type of arrangement) is created and in case that n1,n2 are nonzero they will create a zigzag vector and arrangement is zigzag ,too.

$$C_h = a * \sqrt[2]{{n_1}^2 + {n_2}^2 + n_1 n_2} (5)$$

In this equation, a refers to the distance between carbon atoms and vector and is equal to 0.249 nm. n1,n2 are positive integral numbers that are called Kairalite vector coefficients.
The general equation to calculate carbon nanotube diameter is according to equation 1-2

$$D_{CNT} = \frac{a*\sqrt[2]{{n_1}^2+{n_2}^2+n_1 n_2}}{\pi} (6)$$

The product of fraction $\frac{a}{\pi}$ is equal to 0.0783 . Therefore, the overall equation is as

$$D_{CNT} = 0.0783 * \sqrt[2]{{n_1}^2 + {n_2}^2 + n_1 n_2} (7)$$

Threshold voltage in CarbonNanotube Field Effect Transistor (CNFET)
In CarbonNanotube Field Effect Transistor (CNFET), we can change n1,n2 parameters and consequently carbon Nano tube diameter. so we can adjust and control threshold voltage. This advantage is a reason of superiority of CarbonNanotubeField Effect Transistor (CNFET) to metal oxide field effect transistors.Threshold voltage in CarbonNanotube Field Effect Transistor is calculated using equation 1-4 and based on forbidden band width as:

$$V_{th} \cong \frac{E_g}{2e} = \frac{\sqrt[2]{3}}{3} * \frac{a*V_\pi}{e*D_{CNT}} (8)$$

V_π is the bonding energy of π-π in carbon that is equal to 3.033e.v .e is electron load andD_{CNT} is nanotube diameter. The simple form of this equation is as:

$$V_{th} = \frac{0.43}{D_{CNT}(nm)} v \quad (9)$$

Different structures are designed to reduce the amount of power and increasing speed. Some of these structures used computations including all adders, compressor cells, and multipliers. One of main components in nanotechnology is carbon nanotubes, in recent years ,in different researches carbon nanotubes are used to optimize computation in circuits and different circuits are designed and are mentioned in different journal including *ELEX ، Springer* .In this paper some studies are investigated.,*Elsevier*,*IEEE*&*IEEE*

Literature review

Mahdi darvish in 2017 conducted a research new structure with high performance for 4-2 compressor using CMOS and CNFET technology .in this study a compressor cell 4-2 with higher speed and performance by using CNFETS transistors.

These transistors are suitable for high frequency and low voltage applications. In addition, in this study some common and advanced are investigated and compared.
To evaluate proposed designs,computer stimulation by using CMOS 32 nm , CNFET 32nm are conducted by using different low voltage feeding sources – different temperature and various frequencies and loads. The results of study confirms the superiority of suggested design in terms of energy consumption – delay and delay product –PDP power than other 4-2 compressors .also , the results confirm that this compressor is the fastest 4-2 compressor in different situations.
Also, maleknejad in 2017 conducted a study nasmed multi – threshold gate to access pvt – 2.4 based on MTTG logic and CNFET nanocatbon tubes .Allcell networks in this design are divided into two groups. As a result , the level of voltage decreases and whole structure has lower voltage and temperature changes.
All designs are stimulated by HSPICE synopsy and CNFET 32 technology .in different situations .the results of stimulation show the superiority of the second design ..this design is 55.9% faster and consumption power 27 % less than the second design .also , this design is 16.2% faster and energy consumption is 13.6% less than common BLG designs.In addition , estimates show that the first proposed design occupies the least levels among TLcell circuit.
IN a research done by bagherizade in 2015 entitled designing digital cell counter using transistors in Nano carbontubes, suggested designs include 4, 5, 6, 7.
Stimulations are conducted wing HSPICE in different situations.
Pishvayi (2012) conducted a research entitled 2-4 compressors and showed that 2-4 compressors are the most popular cells with compressed bites and their main implications are in multioperations and multiplier hardware .therefore , performance of 2-4 compressors is influential in increasing implicatedcomputations. The development of these cells is based on XNOR/XOR gates which are equal to three AND/NAND and OR/NOR gates. Division of XOR/XNOR gates in some 2-4 compressors to simpler components results in deletion of some hardware.
In this paper we use such divisions for proposed 2-4 new compressor. Suggested 2-4 compressor and conducted works with HSPICE are done by using standard cell set (CCMOS) in cases that different processors are stimulated. The results of stimulation indicate that the performance of this compressor in terms of delay 17% and product of delay 13% and power 30%.

Research Methodology

Generaly speaking, 2-3 and 2-4 compressors are used for addition. A 2-4 compressor has 5 input and 3 output (like figure)
4 input X1,X2,X3,X4 , cin a have the same value with sum output 4-2 compressor has an input from the previous stage and output from a higher level .a 2-4 compressor can be made by using two additioner like figure 2. Equation (1) is the logic function of 4-2 compressor in which xi shows the main input for addition and ci is the trivial digit from previous stage.

$$x1+x2+x3+x4+ci=Sum+2\times(Carry+Cout)$$

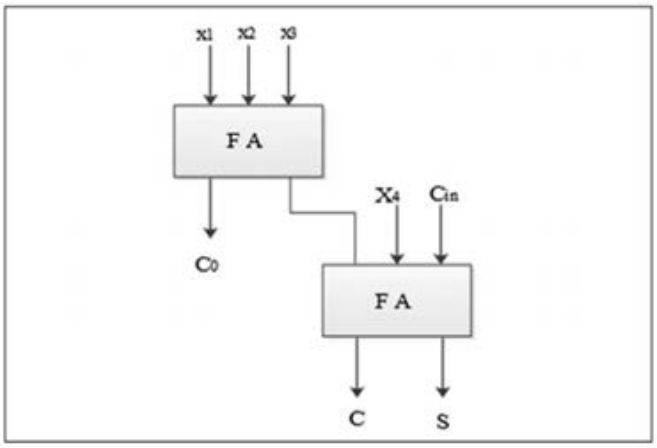

Figure 1: Compressor 4 to 2 using a collector

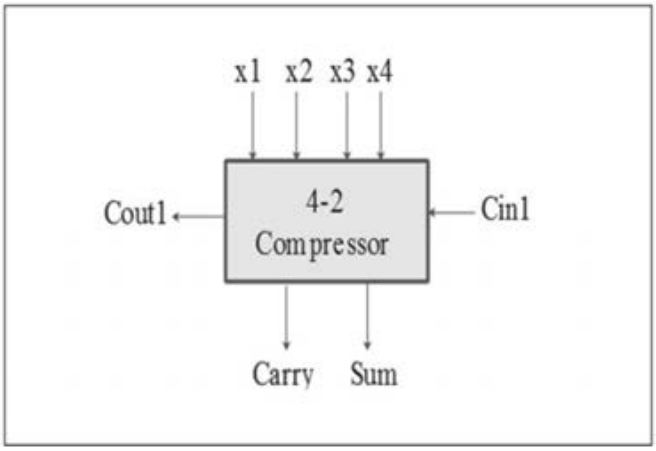

Figure 2 is a block diagram of a compressor 4 to

Non – depenoy to co and input ci guarantees deletion of trivial digit propagation in the process of reducing trivial multiply procuce. although implication of figure 1 results in increasing order of circuit but 4-2 compressor is the main cell in reduction of trivial digits .in all implications , connecting series of XOR/XNOR gates are used to apply XOR with 5 inputs and have 8 outputs.using 2 output consecutive gates causes increasing the signal path lengh and consequently maximum circuit delay.

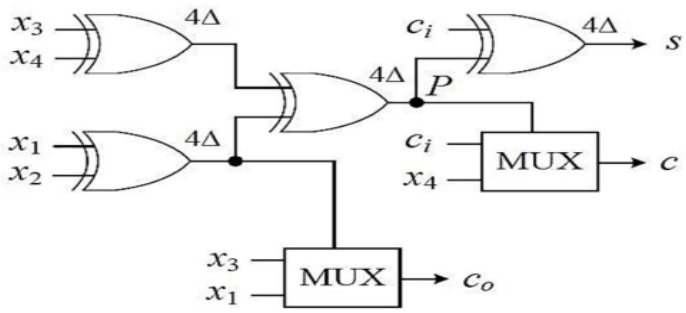

Figure 3:compressor – first proposed design two proposed designs use 27 transistors and 4 not gates from 4XOR input 4 cells and to add fifth input.

We use 2XOR input.as it is shown in block diagram 4 input X1,X2, X3 , X4 are used in reference XOR and then are added by 2 input XOR and produce SUM.
To produce CARRY a multiplexer is used with two inputs X4, cin (p= X1+X2+X3+X4). If p is equal to cin input and p=1 , X4 input is active and p is equal to zero and cin input is active and if p=1 . X4 input is active and p=p= XNOR .the value of count from majority is equal to X1,X2,X3.SOME 4-2 compressor are compared in different threshold interm of CNFET technology .to investigate presented designs , computer stimulations are conducted by using CNFET-32nm.
These stimulations are conducted in different temperatures voltages and frequencies.
For more realistic comparison , the performance of each design is evaluated by using more than 1300 4.2 compressor connections in 54.54 bite multiplier as the test platform using MAGMA instrument. These tests confirm the results of paper aboutesing;e 2-4 compressors . also , in another research by pishvaei improved 2-4 compressor CMOS is presented for parallel multipliers in which three new 2-4 compressors are suggested via improving previous designs and 2 other compressors suggested .based on new interpretations of logical equations .the main point in design is using a signal to produce carrier. All suggested design are evaluated using HSPICE stimulations in different temperatures voltages, loads and changes of process .these experiments show performance improvement in compare with other referencedesigns. Improvement include delay (5%)- POWER(16%) and PDP (26%) . to evaluate studied compressors and new 2-4 compressors , use them to apply parallel multipliers 34.45 bites. Experimental results obtained by MAGMA instrument confirm the results of single 2-4 compressors.

Compressor – first proposed design

In this section , a new efficient 2:4 compressor id presented that is designed based on following equations

SUM = (X1⊕X2⊕X3⊕X4)⊕Cin (10)
Cout = M (X1,X2,X3) (11)
CARRY = (X1⊕X2⊕X3⊕X4)Cin∨ (X1⊕X2⊕X3⊕X4) 'X4 (12)

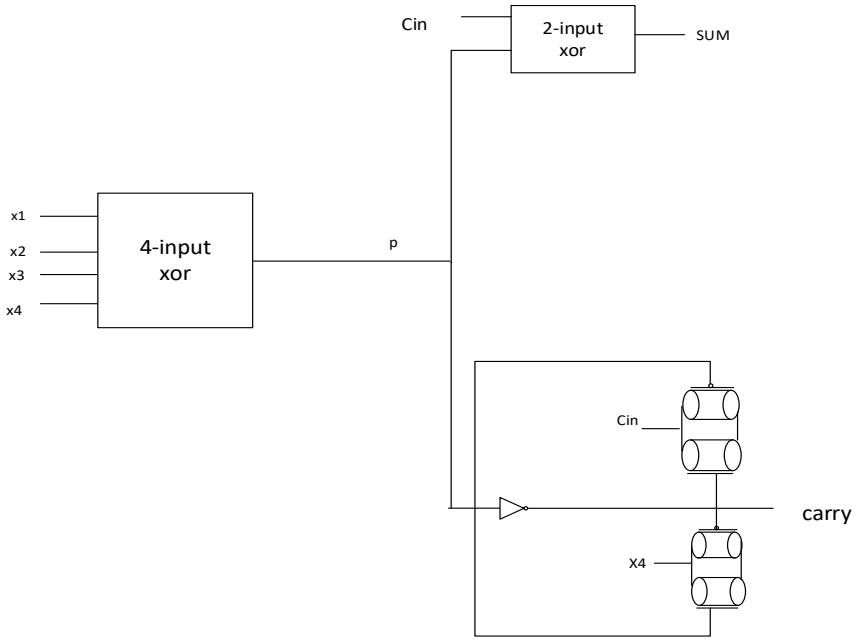

Figure 4-compressor – first proposed design

two proposed designs use 27 transistors and 4 not gates from 4XOR input 4 cells and to add fifth input.
We use 2XOR input.as it is shown in block diagram 4 input X1,X2, X3 , X4 are used in reference XOR and then are added by 2 input XOR and produce SUM.
To produce CARRY a multiplexer is used with two inputs X4, cin (p= X1+X2+X3+X4). If p is equal to cin input and p=1 , X4 input is active and p is equal to zero and cin input is active and if p=1 . X4 input is active and p=p= XNOR .the value of count from majority is equal to X1,X2,X3.SOME 4-2 compressor are compared in different threshold interm of CNFET technology .to investigate presented designs , computer stimulations are conducted by using CNFET-32nm.
These stimulations are conducted in different temperatures voltages and frequencies.

All adders that are used in first proposed design

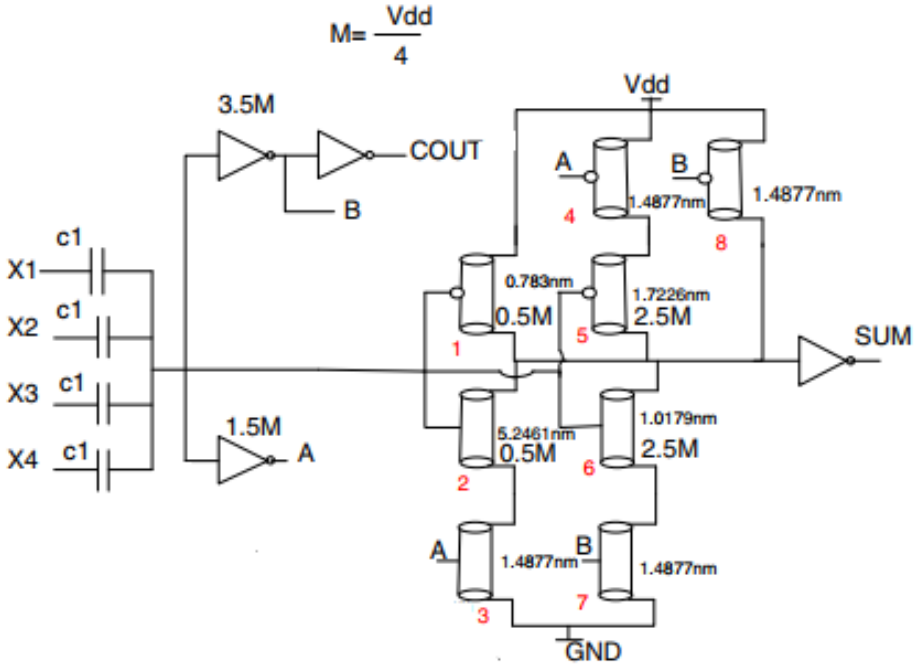

Figure 5- All adders used in the proposed design

In this XOR , 16 transistors are used that have 4 NOT gate. All these adders are based on following equations (13)
SUM= X1⊕X2⊕X3⊕X4 (14)
XOR with two inputs

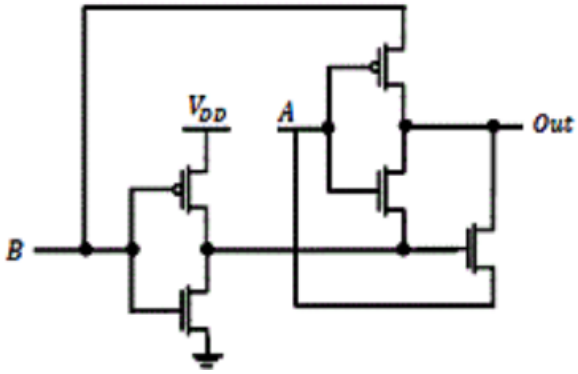

Figure 6- XOR with two inputs

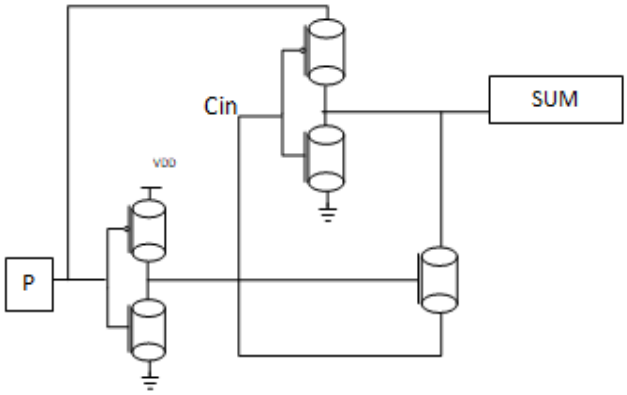

Figure 7- By using XOR,two inputs are added with the fifth input and produce overall SUM.

Overall shape of first proposed design

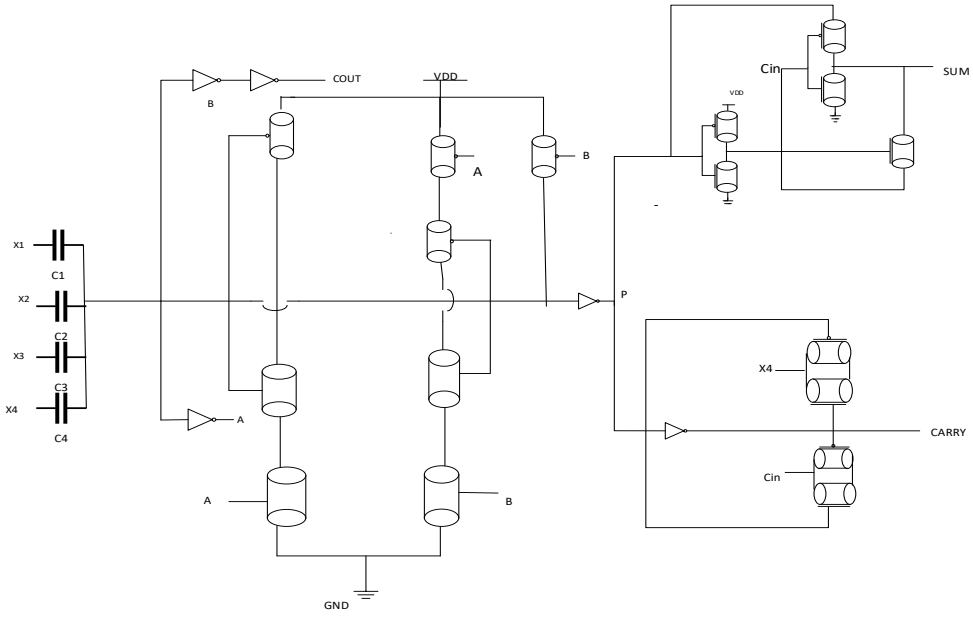

Figure 8. Second proposed 4:2 compressor

The Second proposed 4:2 compressor is shown with following cfaracteristics

SUM=(X1⊕X2⊕X3) ⊕X4⊕Cin (13)
Cout = M (X1,X2,X3) (14)
CARRY=(X1⊕X2⊕X3⊕X4)Cin∨ (X1⊕X2⊕X3⊕X4) 'X4 (15)

In this design , overall SUM is added from three inputs XOR,X1,X2,X3 ,X4 by two inputs XOR and amount of oceral CARRY is obtained by 2X1 multiplier having two inputs cin, x4,. line selection pg p. the amount of count is obtained by majority function

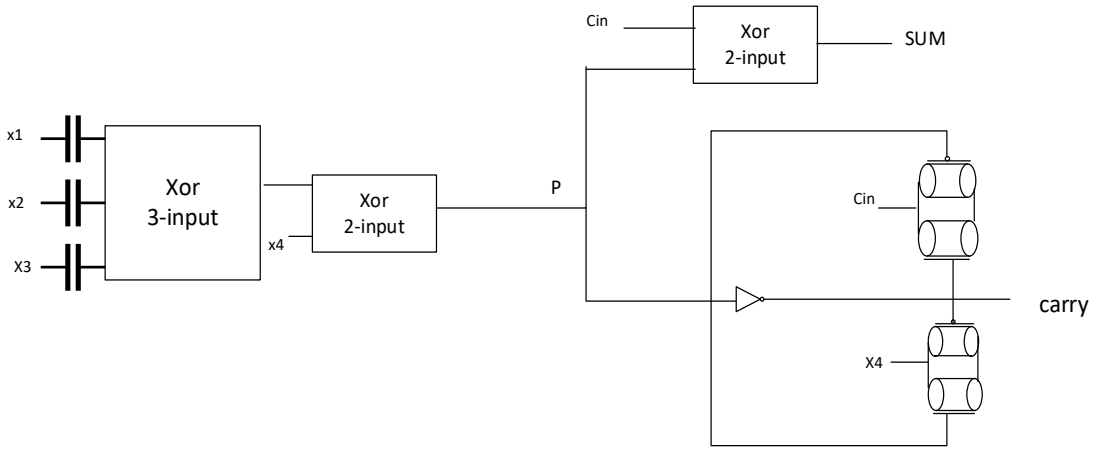

Figure 9- block diagram of 4:2 compressors. the second design

all used adders in the second proposed design

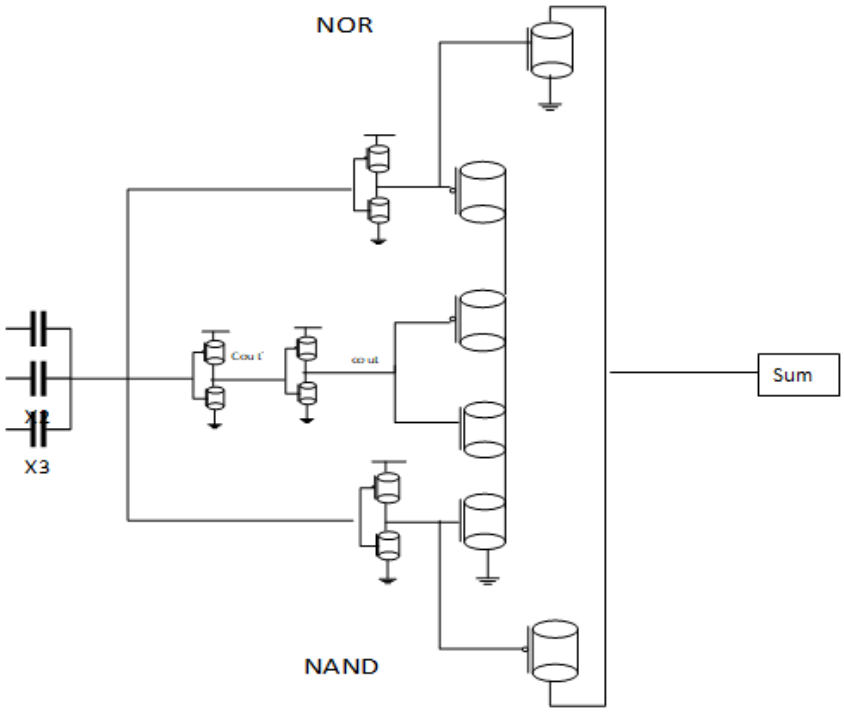

Figure 10- To design this compressor, we use asser having 6 transistors for NOT gates.

Table 1: confirming table of all adders with three inputs

X1 X2 X3	Cout	Cout'	SUM
0 0 0	0	1	0
1 00	0	1	1
0 10	0	1	1
1 10	1	0	0
0 01	0	1	1
1 01	1	0	0
0 11	1	0	0
1 11	1	0	1

According to table ,SUM and Count are similar in 6 situations except two situations for (1,1,1) (0,0,0). When all three inputs are 1 , NAND output is zero.So,PMOS is active if all three inputs are zero.NOR is one and cell is discharged. In 6 situations , sum , is the same as count.

XORWITH 2 inputs for second proposed design is same as XOR for 2 used inputs and is used to add fourth and fifth input

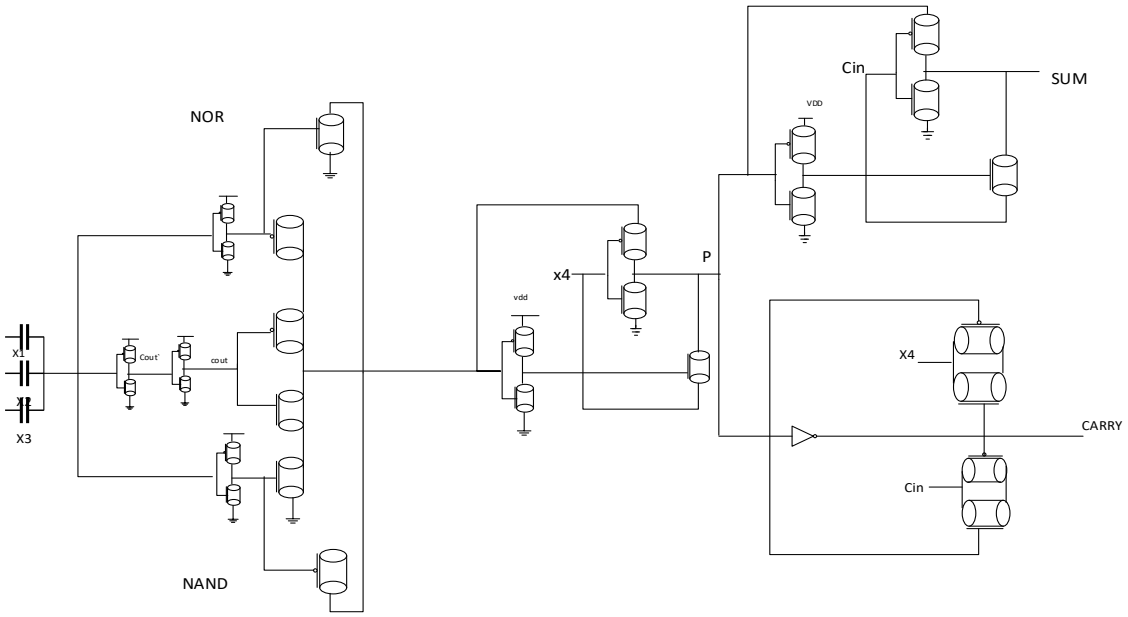

Figure 11-Overall design of 4:2 compressor (second design)

Results

PDP and power parameter charts for suggested designs

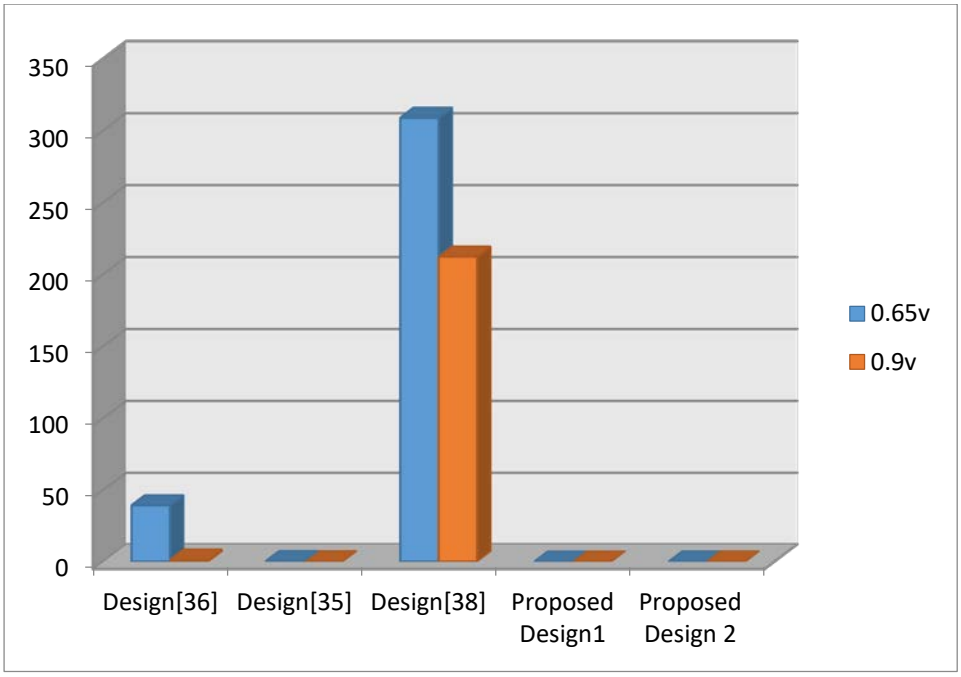

Figure 12- delay parameter chart for suggested designs with previous design in VDD=0.65-0.92.1 ffin 27°C

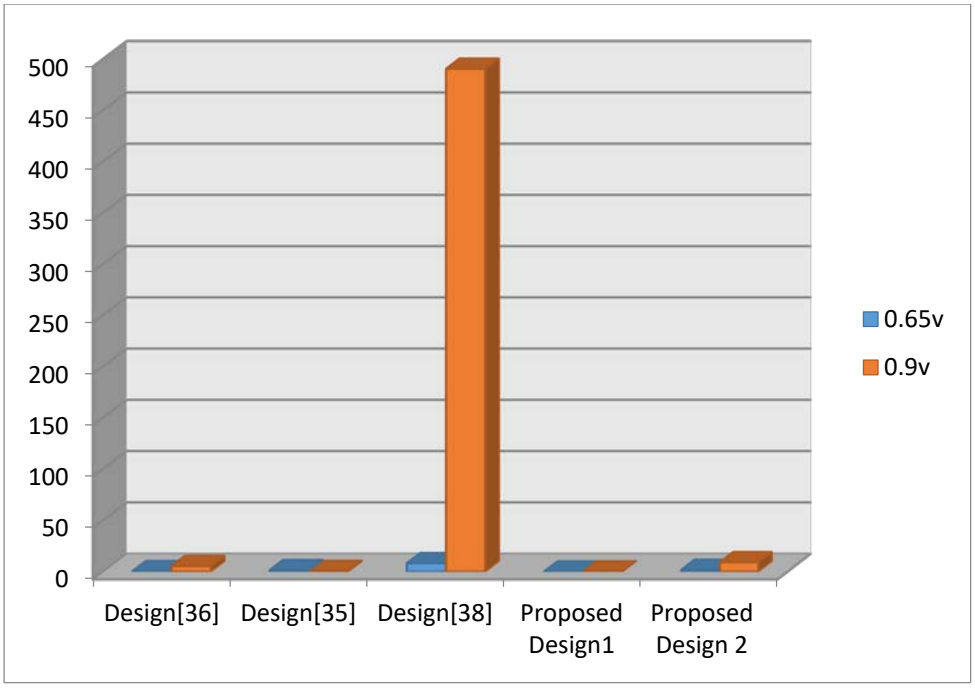

Figure 13- Power parameter chart for suggested designs with previous design in VDD=0.65-0.92.1 ffin 27°C

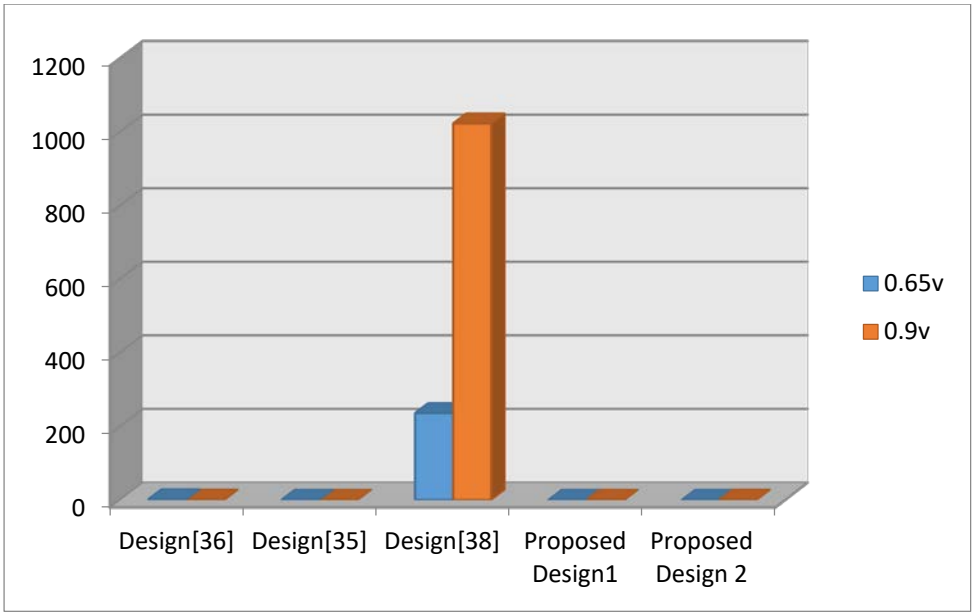

Figure 14: PDP parameter chart for suggested designs with previous design in VDD=0.65-0.92.1 ffin 27°C

Above shown figures indicate that 2 suggested circuits have great performance in terms of speed and power. This results in dramatic reduction of PDP parameter (power multiply by delay). This parameter is so important and researchers try to reduce this parameter.

input and output waves in proposed circuit.

In this section, waves of compressor circuit for two suggested compressors is shown by using CNTFRT in different temperatures and voltages. The shape of waves are extracted by using Hspice stimulator and Cos Mos – scope software.

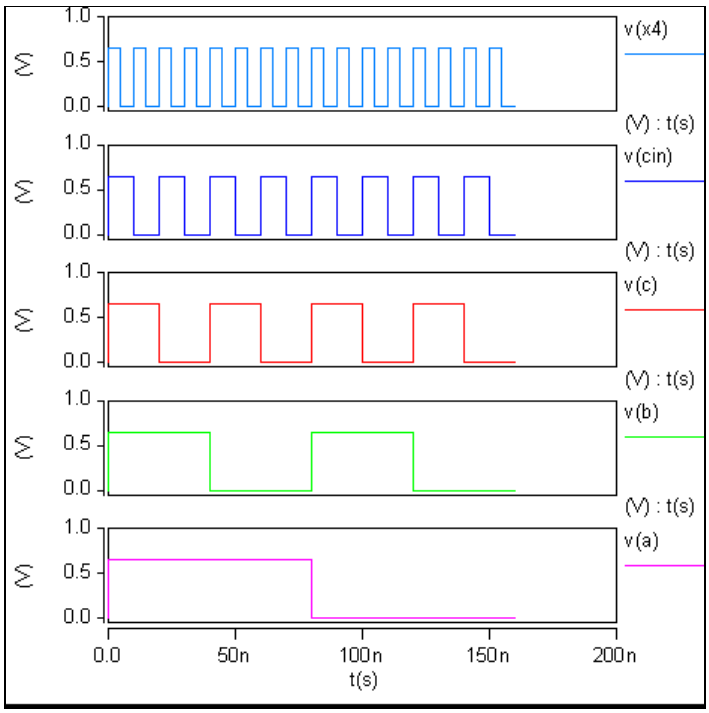

Figure15: Input wave for first compressor design

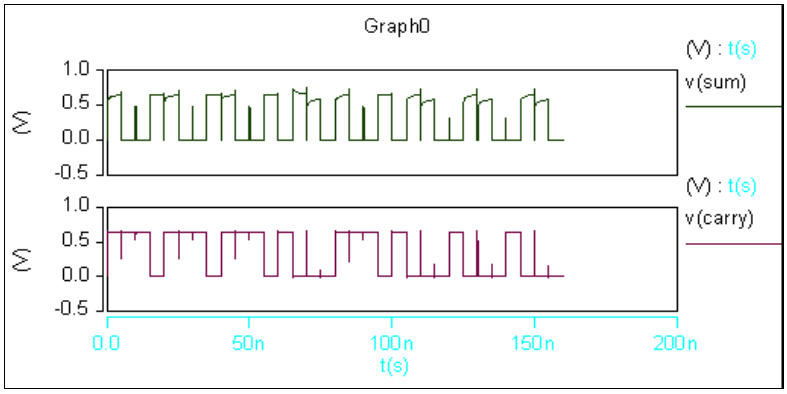

Figure 16: Output wave for first compressor design

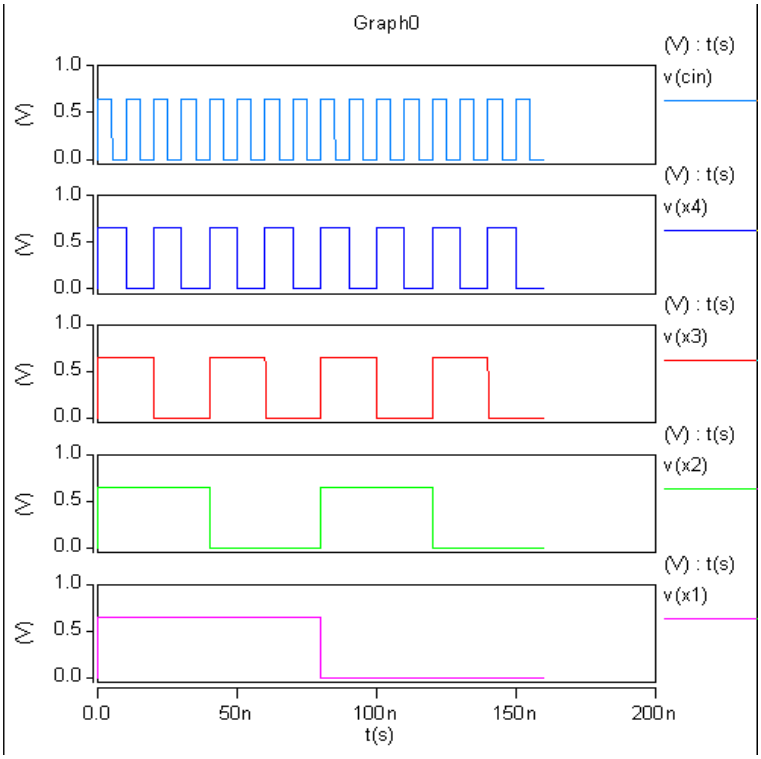

Figure 17: Input wave for second compressor design

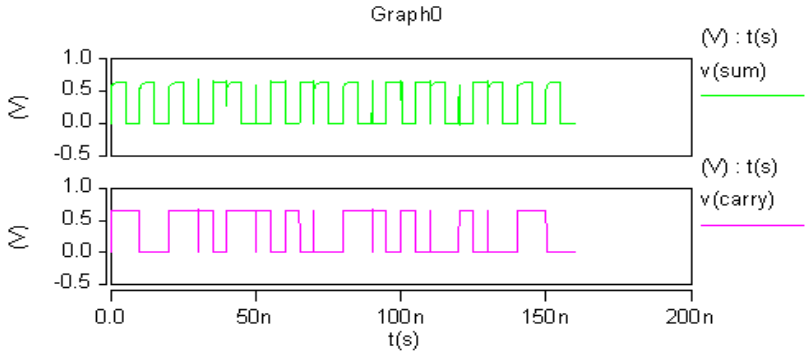

Figure 18: Output wave for second compressor design

Conclusion

Recently, CMOS technology is faced with limitations. Main limitations include physical-usage- heat – technology and economical limitations.
To solve these problems, scientists and researchers look for new alternatives for CMOS technology .therefore, new technologies like QCA – SET- CNFET can be displaced.one alternative technology is CNFET. this technology has some perfect characteristics including unique 1-D band structure – ballistic diversion performance and law off –current, so are similar to CMOS including high compatibility , high current passing.
compressor is stimulated by using synopsy HSPICE 2008 software in different temperatures –voltages and cells. The result of study show the superiority of suggested cell compared to other 4-2 compressors.

Suggestions for further researches

In my opinion, there are many situations for investigation in this field.CNFET technology is one of the best technologies and one can have compressors with lower delay and power by changing internal circuit from 4 to 2 compressors and changing critical paths as well as sum paths. Because of unique monodimensional band structure, connection discreetness deleted and parasites removed ,so , the performance will be similar to ballistic capability of using N,P is another point .as the dimension of carbon tubes increase , threshold voltage changes .higher speed , higher connectivity – lower power – better performance - lower voltage are other characteristics if CNFET. IN THIS Thesis 4-2 compressor with new design and high efficacy is presented by using a multiplexer design.

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