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Designing the Ring-Type Voltage Controlled Oscillator

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Abstract: *A voltage controlled oscillator (VOC), in fact, is a generator of adjustable frequency. A VOC is used as a key part in the phase lock ring, which is a system that generates a sustained oscillating signal. Since the digital electronics industry needs a growing increase of performance in speed, it is necessary that the VOCs generate the signals in higher frequencies. But, as the frequency increases, the VOC phase noise decreases. Even though there are two main types of VOCs i.e. ring and capacitive-inductive types, in this research, the ring oscillator is designed and simulated using the Dual-gate transistors. The results showed that, compared to MOSFET transistors, frequencies could be generated using the dual-gate transistors. Then, various signals were generated using the op-amp and frequency divider and also using the ring oscillator. Finally, three outputs were weighted and summed and it was shown that oscillations with three times of frequency could be generated using the weighted sum of the phase shift oscillator output.*

Keywords: *Voltage Controlled Oscillator, Ring oscillator, Dual-gate transistor, Frequency divider.*

INTRODUCTION

In recent years, the efforts for downsizing the transistors have become very important (Venkateshwar and Jagadesh, 2005). Among the most reasons for making the transistors smaller are decreasing the costs, reducing the power consumption, increasing the speed and making the electronic pieces more compact and also lighter. Despite these advantages, some physical restrictions appear in downsizing the transistors and some unwanted effects such as threshold voltage change, the increase leak current, potential barrier decrease by drain induction, decrease of sub-threshold slope, the decrease switching speed and limitation on the drift of electron specifications will be observed in transistor's behavior that some of these effects are expressed as Short-Channel Effects (Venkateshwar and Jagadesh, 2005; Ajay Kumar Singh, 2010). In fact, due to these short-channel effects, downsizing the transistors has faced some challenges. In order to dissolve this problem, dual-gate MOSFET transistor could be used. In (Venkateshwar and Jagadesh, 2005) for dual-gate MOSFET transistor that the gates have different biases, a model has been presented for drain current and threshold voltage for long channel MOSFETS that in it, a threshold voltage is defined for each gate and by changing the gate bias this value will no longer change. Then, for determining the channel potential, the two-dimensional Poisson equation by a combination of superposition principle and evanescent mode has been used and for modeling the effects of short channel, the threshold voltage and sub-threshold slope have been used. In (Ajay Kumar Singh, 2010) work has been performed for finding the answer to the one-dimensional Poisson equation in dual-gate MOSFET in which, the channel has been considered without impurity or with low impurity and

only the dynamic loads have been considered in Poisson equation. In (Munteanu and Autran, 2009) the existing methods for modeling the drain current in dual-gate and single-gate Silicon on Insulation (SOI) MOSFETS have been compared. In (Reyboz, Rozeau and Poiroux, 2009), by comparing the dual-gate MOSFETS with single-material gate and dual-material gate, the improvement of the effects of the short channel using two materials for the gate has been pointed out. Also, the decrease in the effects of the short channel due to the existence of a step function in the superficial potential has been investigated. In (Saheli, Sounak and Subir, 2012), the XOR and XNOR digital gates are designed and implemented using dual-gate MOSFETS. The results showed that the designed circuits with these transistors have higher speed and lower power consumption compared to the common MOSFET transistors. In (Omar, Ishiang and Yi-Chi, 2014), a dual-gate MOSFET is studied for low consumption and low voltage applications. In (Arun Samuel and Balamurugan, 2014) the effect of multi-material gates on the effects of the short channel in Silicon on Insulation (SOI) MOSFETS have been studied and various transistor parameters are compared. In (Changyong Zheng et al., 2013), in order to estimate the potential dissolution from the two-dimensional Poisson equation in the channel, the combination of the evanescent mode and parabolic approximation is used. In (Wei and Cheng, 2013) the analog and high-frequency performance of dual-gate transistors in the 20 nm technology has been studied using the Silvaco software. Due to the presented content, in this design, using the dual-gate transistors that are proposed in recent years, a ring-structured oscillator will be designed for the first time that has as low as possible power consumption for phase noise performance and high generated frequency precision. In addition, the swing and sustainability of the ring will be acceptable and proper for telecommunication applications. Therefore, in designing the oscillator, we will try to present the innovations and new ideas for increasing the precision and signal to noise ratio in such to minimize the power consumption as low as possible so that the ring complexity would not be higher than the similar structures. Therefore, according to the mentioned content, the main objective of this research is to design an oscillator controlled by ring-type voltage.

Research Methodology

In this research, the design and simulation of the ring oscillator are addressed using dual-gate transistor. For this purpose, we need a model to simulate this transistor. Since we use the HSPICE software for simulation, we must have a model in PSPICE level for a dual-gate transistor. In (Shi Cheng et al., 2004) a model has been presented for dual-gate transistor that we use this model for simulating the dual-gate transistor. Also, for comparing the results, the design will be carried out in 0.18 um CMOS technology and the results will be compared. The utilized model for the dual-gate transistor is as follows:

```
+ WKFG=4.60
+ WKBG=4.60
+ NSF=1e10
+ NSB=1e10
+ TOXF=2n
+ TOXB=2n
+ TSI=10.0n
+ NBODY=1E15
+ UO=1400
+ THETA=1.0
+ VSAT=1e7
+ VO=0
+ BLIM=0
```

+ QMX=1.0
+ QMD=1.0
+ NDS=1E20
+ JRO=1E-11
+ M=1.5
+ SEFF=1E5
+ SCEB=0
+ DL=1e-9
+ LES=0.0n
+ LED=0.0n
+ RD=100E-6
+ RS=100E-6
+ SFACT=5
+ WFACT=5
+ SO=1
+ BJT=0
+ DG=1
+ GAMMA=0.06
+ KAPPA=0.11
.MODEL PDG PMOS LEVEL=10
+ WKFG=4.60
+ WKBG=4.60
+ NSF=1e10
+ NSB=1e10
+ TOXF=2n
+ TOXB=2n
+ TSI=10.0n
+ NBODY=1E15
+ UO=500
+ THETA=0.8
+ VSAT=7e6
+ VO=0
+ BLIM=0
+ QMX=1.0
+ QMD=1.0
+ NDS=1E20
+ JRO=1E-11
+ M=1.5
+ SEFF=1E5
+ SCEB=0
+ DL=1e-9
+ LES=0.0n
+ LED=0.0n
+ RD=100E-6
+ RS=100E-6
+ SFACT=5
+ WFACT=5

+ SO=2
+ BJT=0
+ DG=1
+ GAMMA=0.06
+KAPPA=0.11

Findings

In this research, at first, we will perform the design and simulation of simple digital circuits using dual-gate transistors. The model used for simulation is the presented model in (Shi Cheng et al., 2004) that is a comprehensive and efficient circuit level for dual-gate transistors. Figure (1) shows the results of simulation of dual-gate transistors with HSPICE. For comparison, the results of the simulation of this circuit using the 0.18 um CMOS technology are also plotted. The power consumption graph for both the dual-gate and MOSFET transistors is plotted in Figure (2). It could be observed that the dual-gate transistor has a very much lower power consumption compared to the MOSFET. The maximum power of the dual-gate transistor is about 400 μW while the MOSFET transistor consumes more than 80 mW of power.

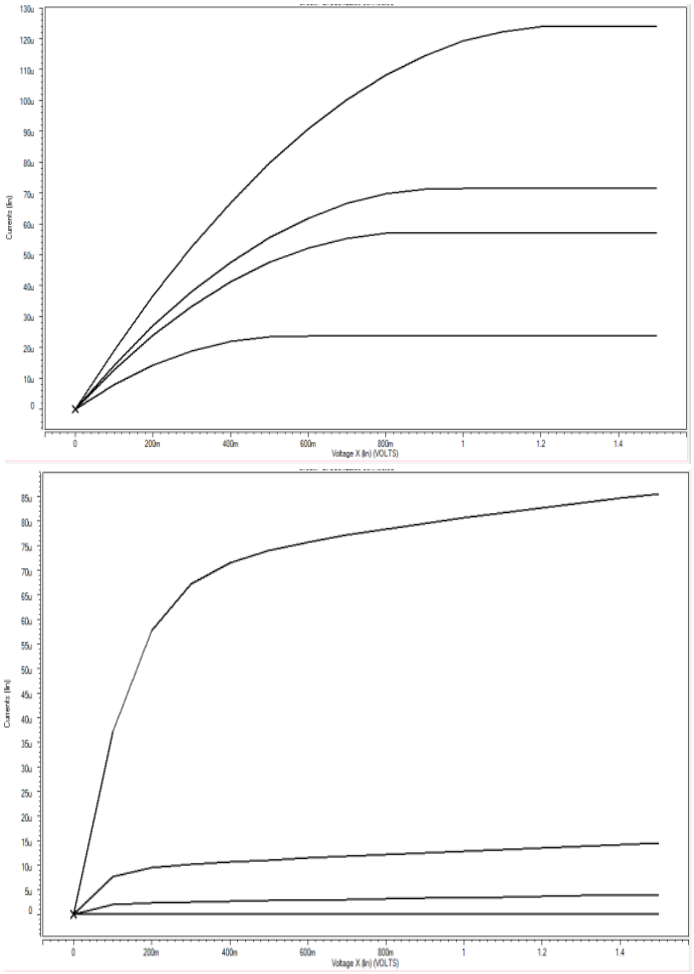

Figure 1: The voltage-current graph of the dual-gate transistor (up) and MOSFET transistor (down).

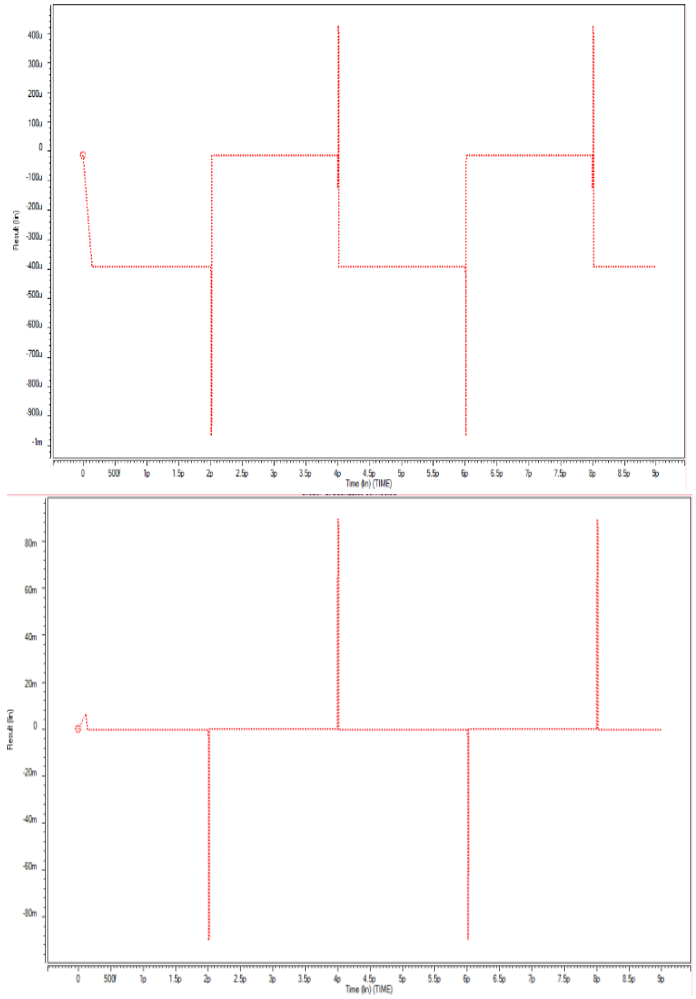

Figure 2: The power consumption graph of the dual-gate transistor (up) and MOSFET transistor (down).

Designing the ring oscillator with dual-gate transistor

Figure (3) shows the results of the simulation of a three-stage ring oscillator using the HSPICE software for both the dual-gate and MOSFET transistors. All the three outputs of the ring oscillator are shown in this figure. It could be observed that each of the outputs have phase deference with each other. In addition, the generated oscillation frequency using the dual-gate transistor is very much higher than the MOSFET transistor. The oscillator that is designed using the dual-gate transistor has 35 GHz frequency, while the transistor that is designed by the MOSFET transistor, has 2 GHz frequency. Therefore, using the dual-gate transistor, the oscillations with very much higher frequency could be generated compared to the MOSFET transistor.

The shape of the final output wave of the three-stage ring oscillator for dual-gate technology is shown in Figure (4). From now on, we only perform the design using the dual-gate transistor. From the figure, it could be observed that a sinusoidal graph is generated. The oscillation frequency of this oscillator is about 35 GHz.

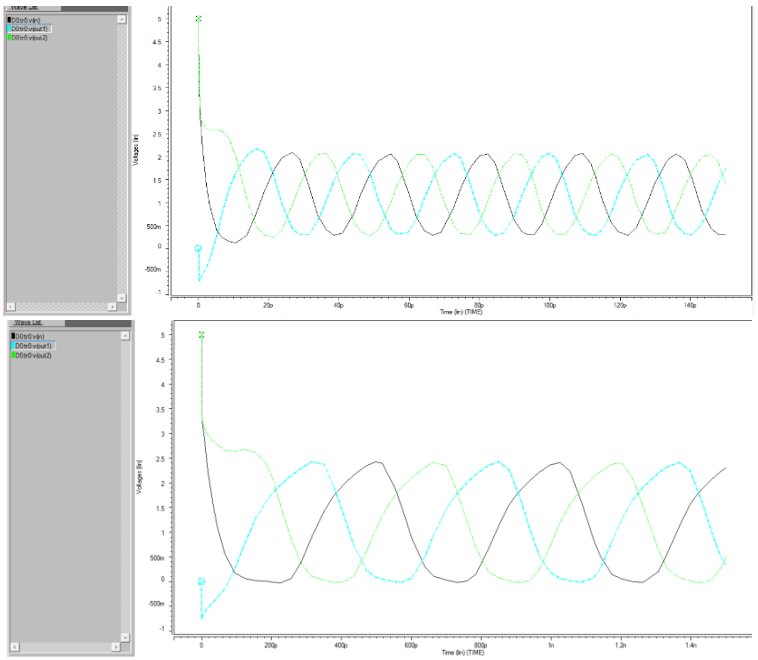

Figure 3: Three various outputs of three-stage ring oscillator using the dual-gate transistor (up) and MOSFET transistor (down).

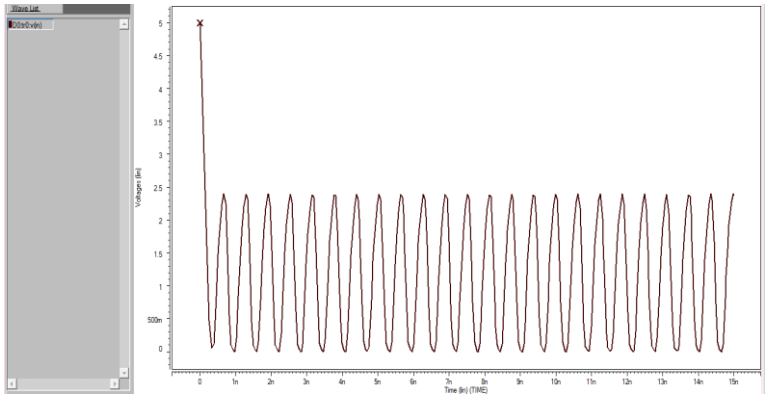

Figure 4: Final output of the three-stage ring oscillator.

The output spectrum of the three-stage ring oscillator is shown in Figure (5).

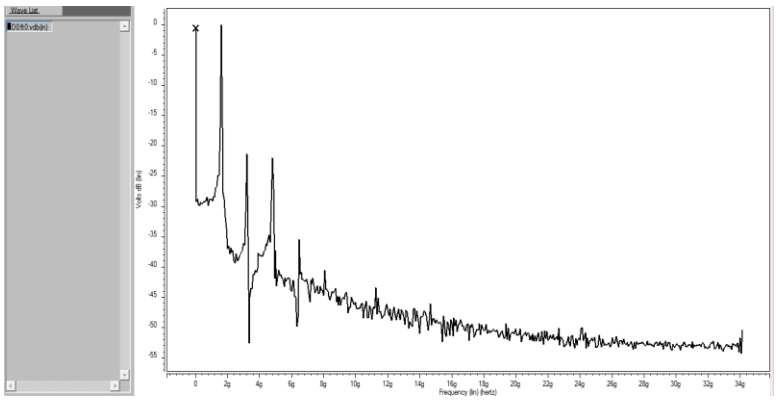

Figure 5: output spectrum of the three-stage ring oscillator.

In order to show the effect of the number of stories on the oscillator performance, a five-stage ring oscillator will be designed and simulated using the HSPICE. The results of this simulation are shown in Figures (6) and (7). The oscillation frequency of this oscillator is about 0.9 GHz that is lower compared to the three-stage ring oscillator. Therefore, increasing the number of stories results in the decrease of oscillation frequency. This is because with the increase in the number of the stories, the delay between the input and output increases and therefore the frequency decreases. The graph of the five-stage oscillator output spectrum is shown in Figure (8). The oscillation frequency for this oscillator is about 20 GHz.

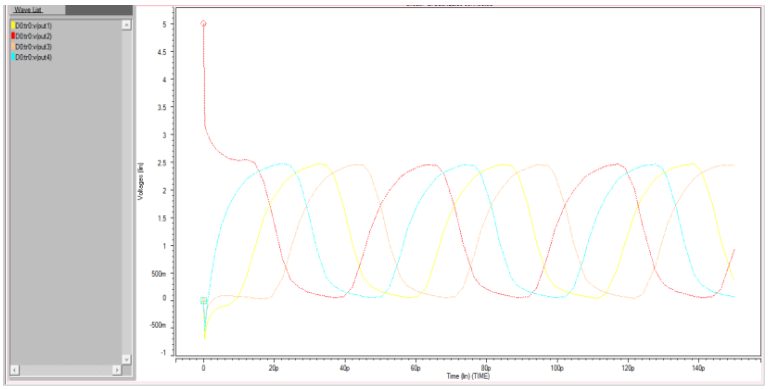

Figure 6: Various outputs of the five-stage ring oscillator.

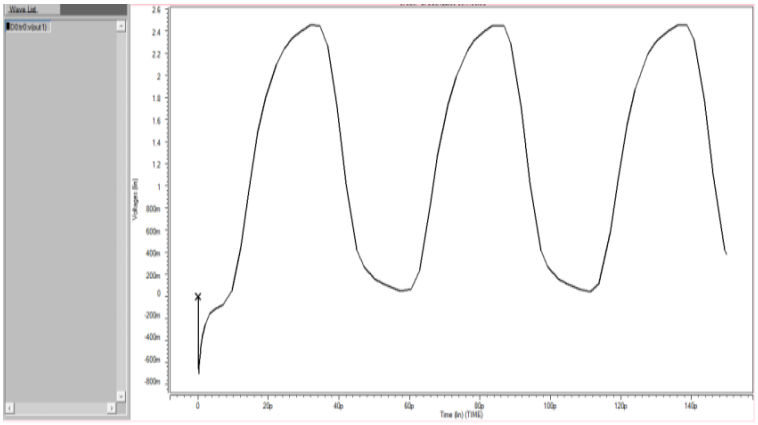

Figure 7: Final output of the five-stage ring oscillator.

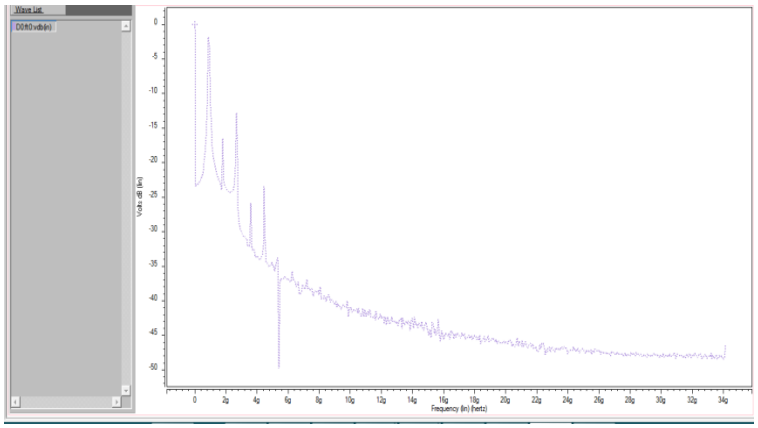

Figure 8: Outputs spectrum graph of the five-stage ring oscillator.

As we observed in previous results, the ring oscillator has outputs with various phases. These outputs could be summed together and generate different signals.

Designing the op-amp

There is a need for an op-amp or operational amplifier to use the weighted summation method for generating various signals. For this reason, in this research, an op-amp is designed and simulated and using this op-amp, the collector is designed and then using this collector and ring oscillator, we will generate various signals.

The results of this op-amp simulation are shown in Figure (10). This op-amp has the unit cutoff frequency equal to 222 MHz, phase limit of 66.7 degrees, voltage efficiency of 36000 and power consumption of 5 mW that are very acceptable and proper results. Using this op-amp, the weighted collector circuits will be designed.

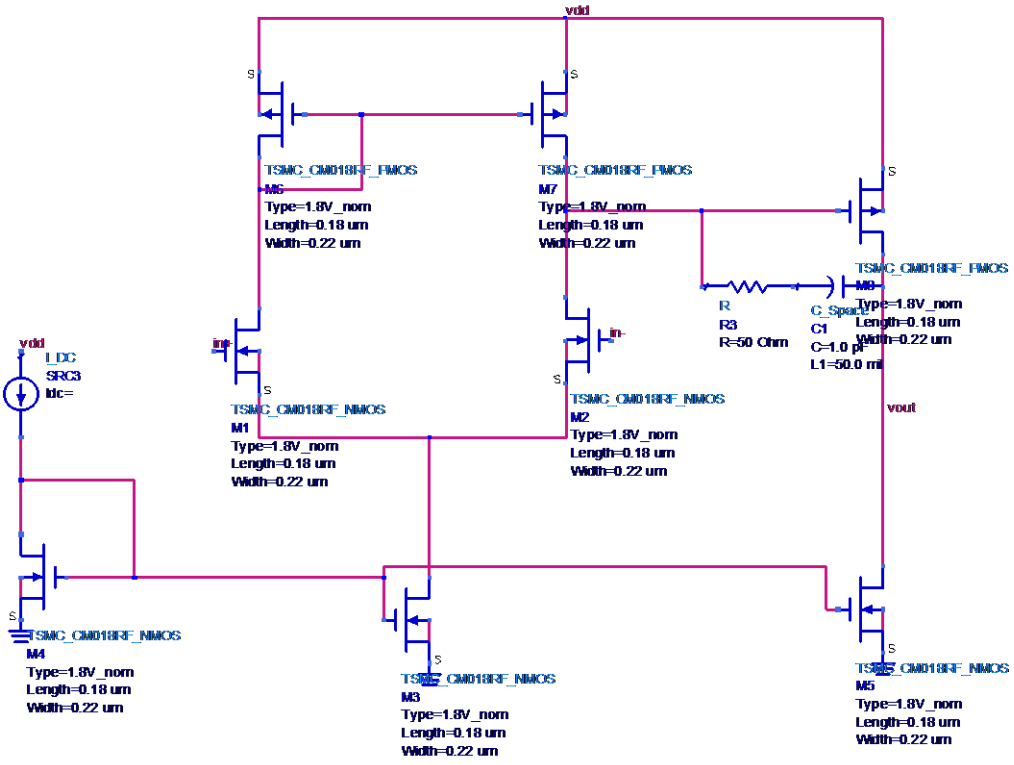

Figure 9: The designed two-stage internal op-amp circuit.

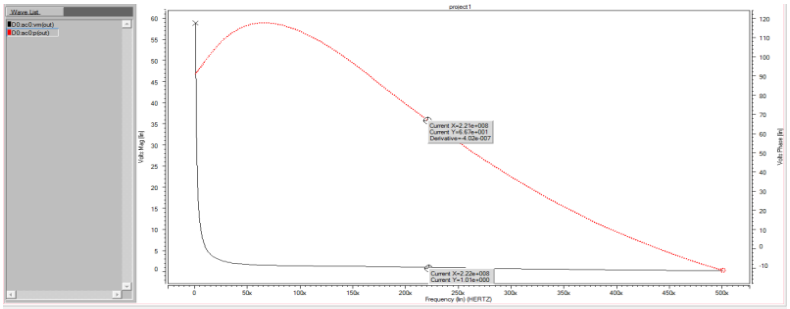

Figure 10: The result of two-stage op-amp simulation.

Figure (11) shows circuit having feedback using an op-amp. Here, the op-amp circuit is shown using its electronics symbol.

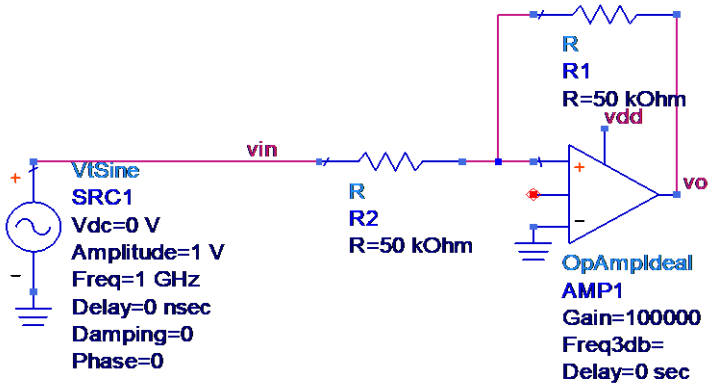

Figure 11. A circuit having feedback using an op-amp.

The simulation results of this circuit in HSPICE is shown in Figure (12). This circuit is designed for the closed ring efficiency of 10. Figure (13) shows a collector circuit using this op-amp. Using this circuit and various weights, different signals could be produced. For showing this subject, we will simulate this circuit with various sinusoidal inputs with various frequencies and amplitudes. Figure (14) shows the results of this simulation. It is clear in this figure that a triangular waveform could be generated using various sinusoidal signals with various amplitudes and frequencies. In the same way, various signals with various waveforms could be generated.

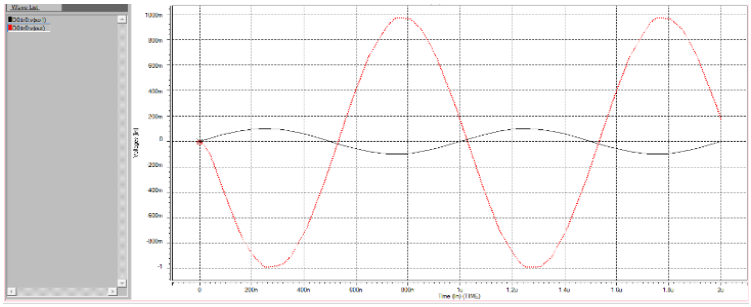

Figure 12: The result of two-stage op-amp simulation having feedback.

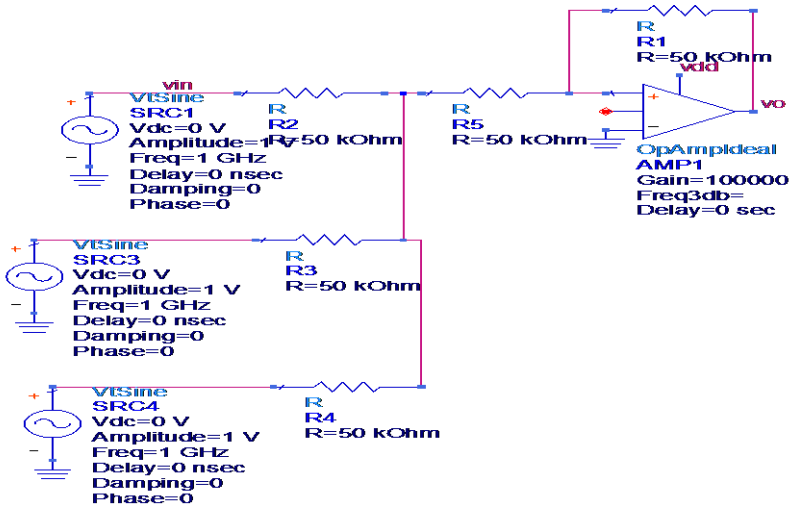

Figure 13: The weighted collector circuit using the op-amp.

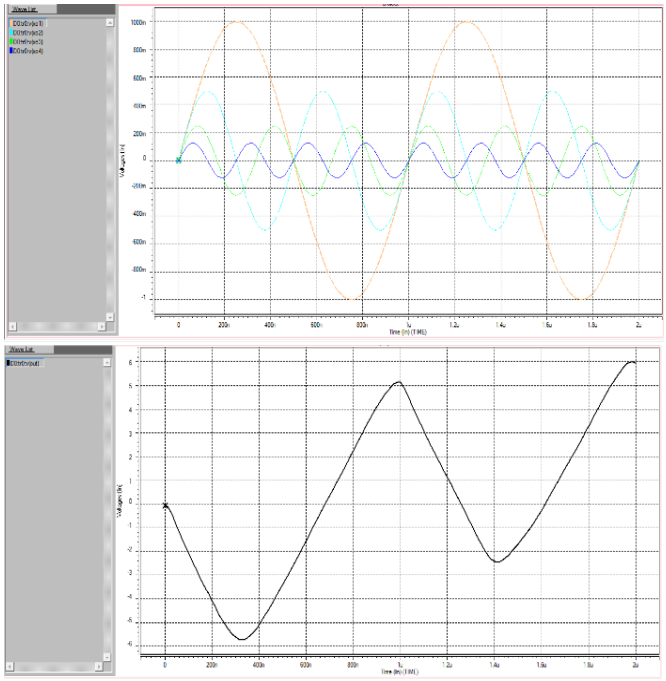

Figure 14: The result of the simulation of the weighted collector circuit using the op-amp.

- **The weighted summation method for signal generation**

In this section, a ring oscillator is described using the weighted summation method of ring oscillator outputs. Figure (15) shows the ring oscillator with the weighted summation method for the outputs.

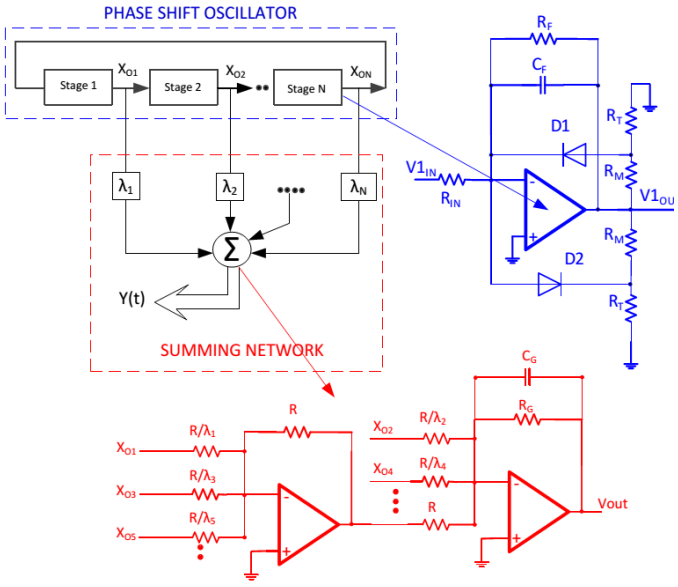

Figure 15: Ring oscillator with a weighted summation method of outputs.

This circuit will be designed and simulated using the op-amp designed in the previous section. Figure (16) shows the results of this circuit simulation. This circuit will be simulated and optimized for various weights. Figure (17) shows the result of this simulation for identical weights. It could be observed in this figure that the output is saturated. Figure (17) shows the output result for the optimized weights.

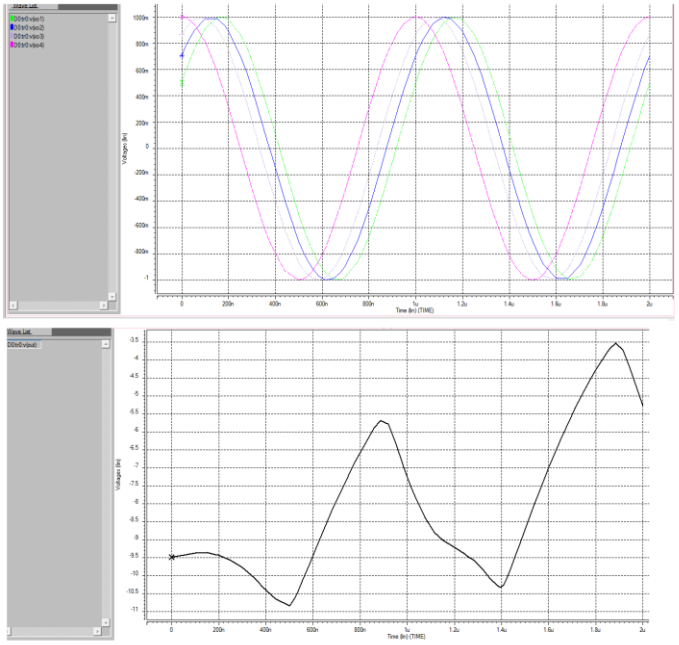

Figure 16: The results of the circuit of Figure 15 simulation for identical weights.

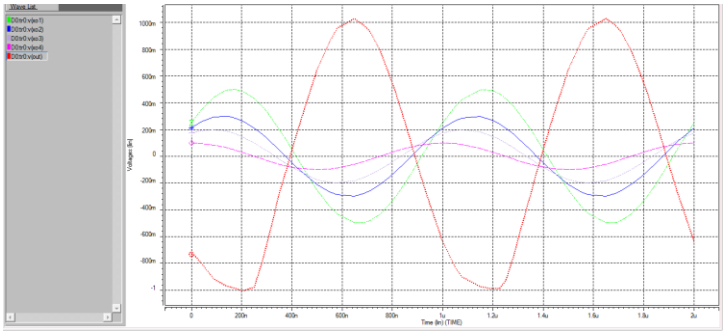

Figure 17: The simulation results of the circuit in Figure 15 for optimized weights.

Figure (18) shows the phase noise graph of the proposed oscillator. It could be seen in this figure that this oscillator has very small noise and equal to -82dBc/Hz.

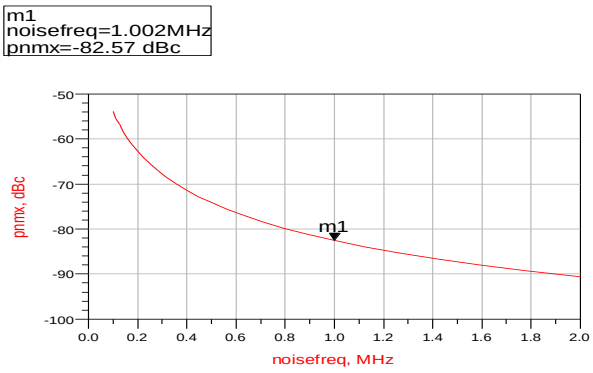

Figure 18: The graph of phase noise of the proposed oscillator with optimized weights.

- **Designing the frequency divider**

There is a need for signals with various frequencies in order to generate a different signal by the weighted summation method. Therefore, here an adjustable frequency divider circuit is designed.

In this circuit, by changing the load resistances the output frequency could be regulated. A sinusoidal frequency with 10 GHz frequency is applied to this circuit. Figures (20) and (21) show the input and output waveform for this frequency divider, respectively.

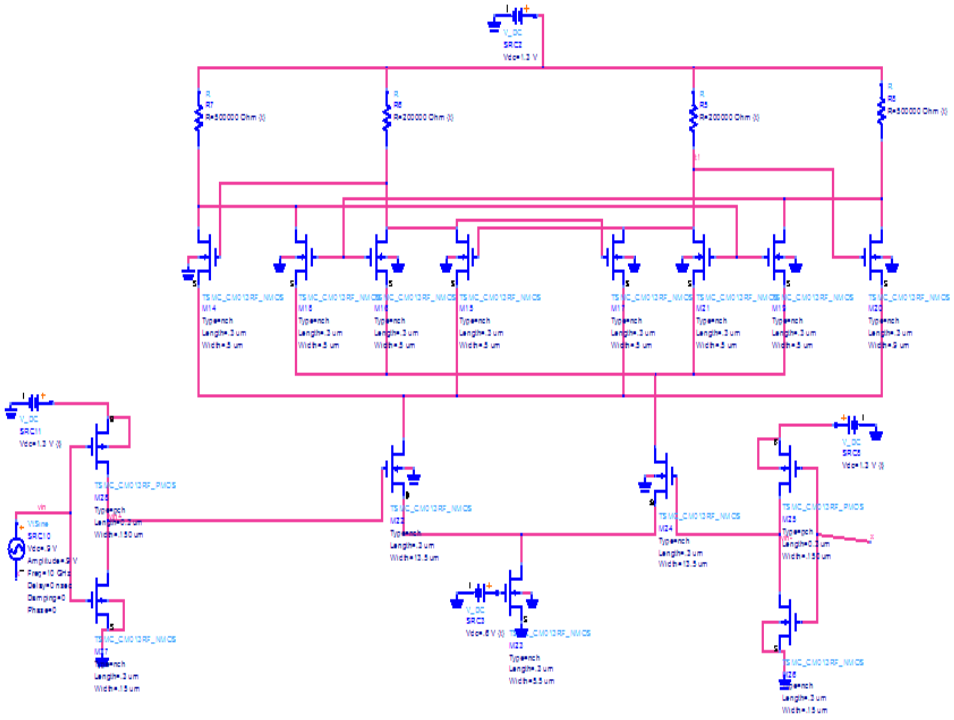

Figure 19: High frequency, frequency divider circuit.

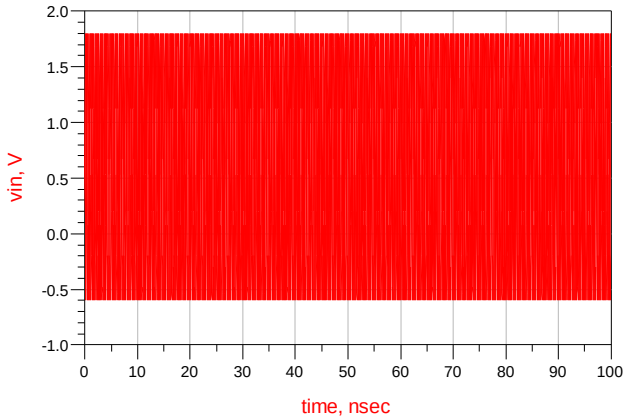

Figure 20: Input diagram of the frequency divider.

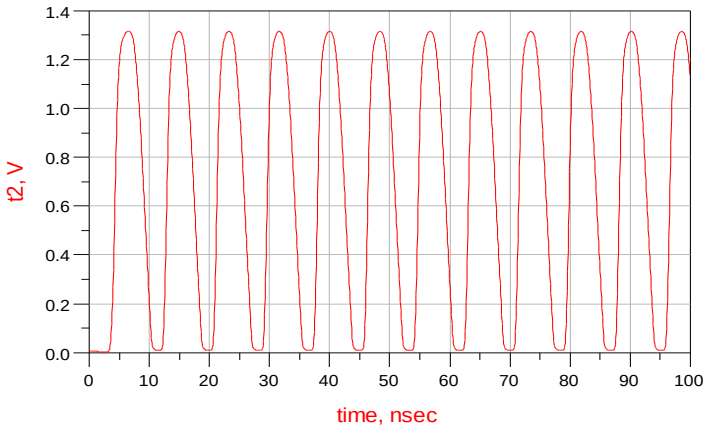

Figure 21: Output diagram of the frequency divider.

This circuit gets a sinusoidal input with 10 GHz of frequency and divides the input frequency and a function of R5, R6, R7 and R8 resistances and generates an output signal with the frequency of 204 MHz. Table (1) shows the power consumption of this frequency divider. Therefore, this frequency divider consumes only 16 µW of power. As was described, this method is designed in such a way that the output frequency is sensitive to the load resistance. By changing the load resistance, the output frequency could be changed. To show this subject, we will simulate the previous divider for various resistances. Here, we will only change the last resistance on the right side. Figures (22) to (24) show the output wave for various resistances. It is clear from these results that by changing the resistance, the output frequency can be changed.

Table 1: Power consumption of the frequency divider in Figure 30.

freq	power
0.0000 HZ	1.657E-5 / 0.000
5.000 HZ	8.962E-7 / 107.951
10.00 HZ	1.459E-7 / -6.015
15.00 HZ	4.903E- 8 / 118.506
20.00 HZ	1.714E-8 / 14.079
25.00 HZ	1.862E-8 / 66.182

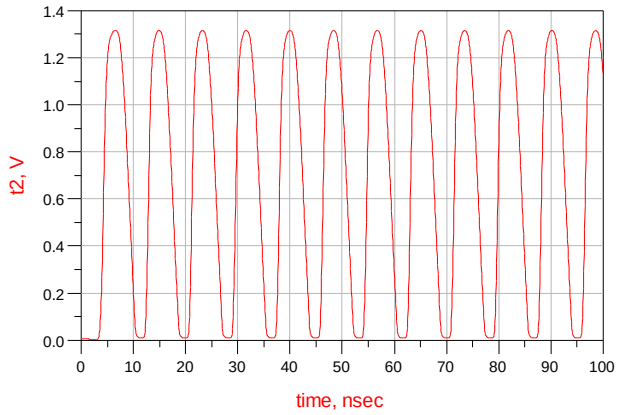

Figure 22: The output of the frequency divider for R5 = 900 K, Frequency = 118 MHz.

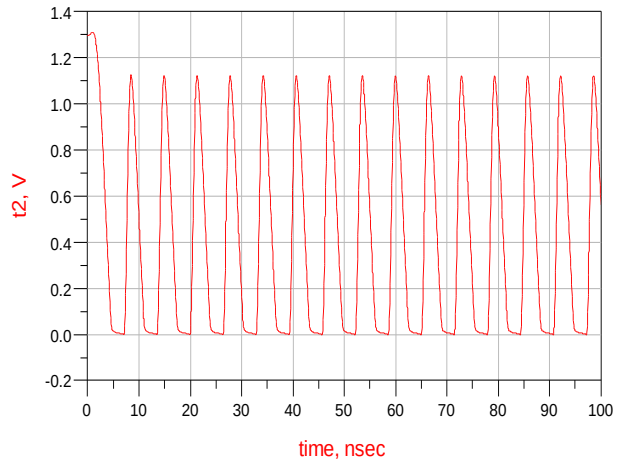

Figure 23: The output of frequency divider for R5 = 100 K, Frequency = 156 MHz.

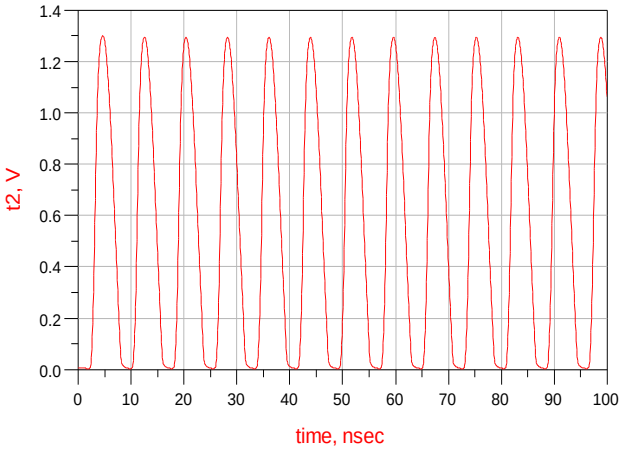

Figure 24: The output of frequency divider for R5 = 500 K, Frequency = 131 MHz.

The following table shows the frequency changes versus load resistance.

Table 2: Frequency change versus resistance.

F (MHZ)	R (K ohm)
156	100
172	200
134	300
147	400
131	500
128	600
120	700

- **Designing the proposed ring oscillator circuit**

Here, a proposed circuit for delay cell design and ring oscillator design is presented. Figure 4-28 shows the circuit schematics of the proposed plan. Here, three delay cell is used for ring oscillator design that as a result, three different signals with identical frequency are generated that have phase differences. Figure 4-29 shows the output of this ring oscillator.

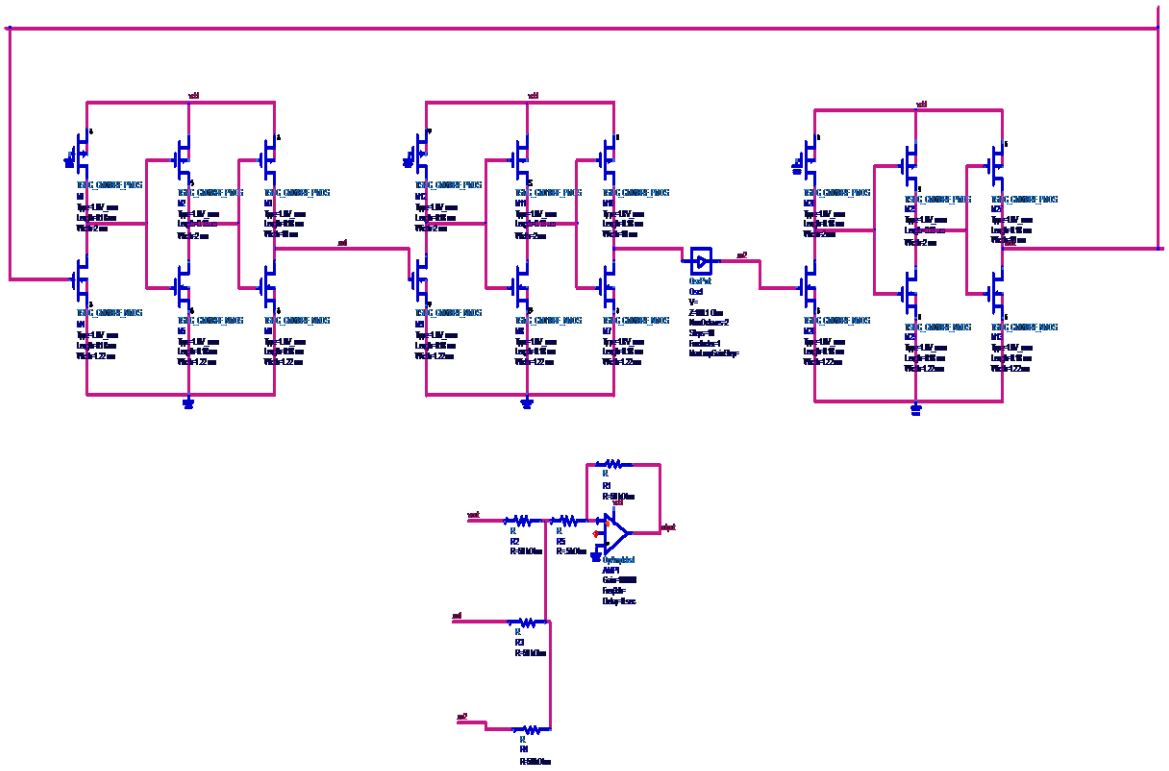

Figure 25: The proposed ring oscillator circuit with the weighted collective circuit.

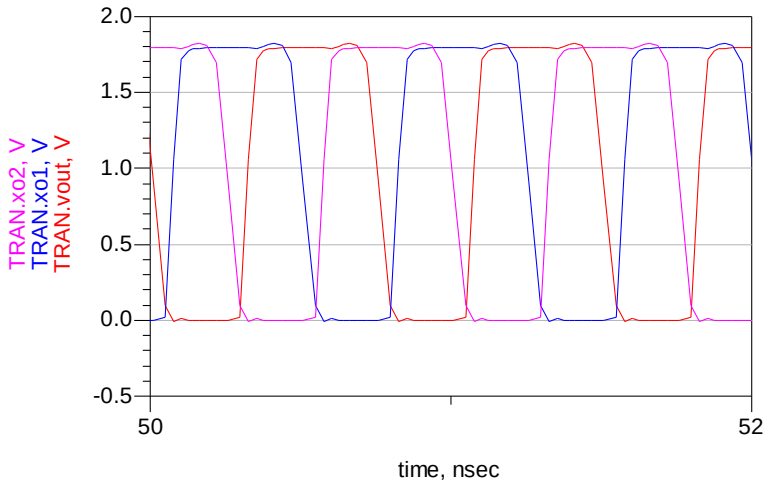

Figure 26: The waveforms of the three proposed ring oscillators.

Figure (27) shows the output of the weighted summation of the proposed circuit. Using more stories and proper weights signals with various shapes could be generated.

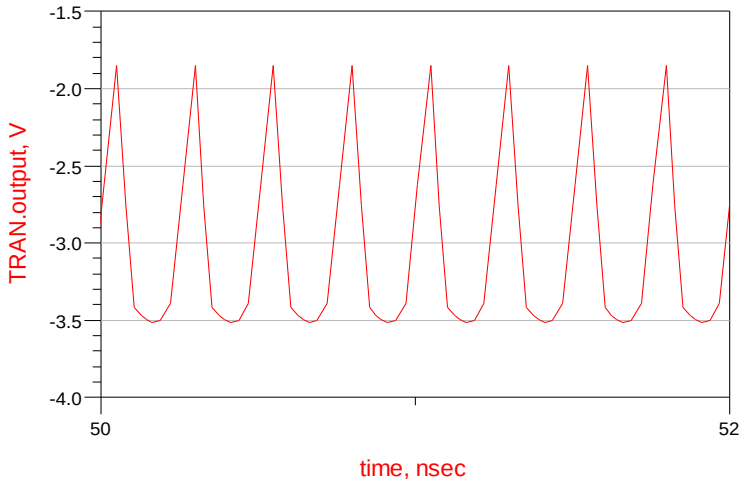

Figure 27: The output of the weighted summation of the proposed circuit.

Now, using the frequency divider circuit, and using the proposed ring oscillator, the signals with various frequencies will be designed and the signals with various frequencies will be weighed summed so the final output would be generated. Figure (28) shows the circuit schematics and Figure (29) shows the output with various frequencies and Figure (30) shows the output obtained from the weighted summation. The oscillation frequency of this output is equal to 21 GHz that is almost three times of phase shift oscillator oscillation frequency. In fact, here, using the designed frequency divider in the previous section, various frequencies will be generated. These frequencies will be weighed summed together so different signals will be generated.

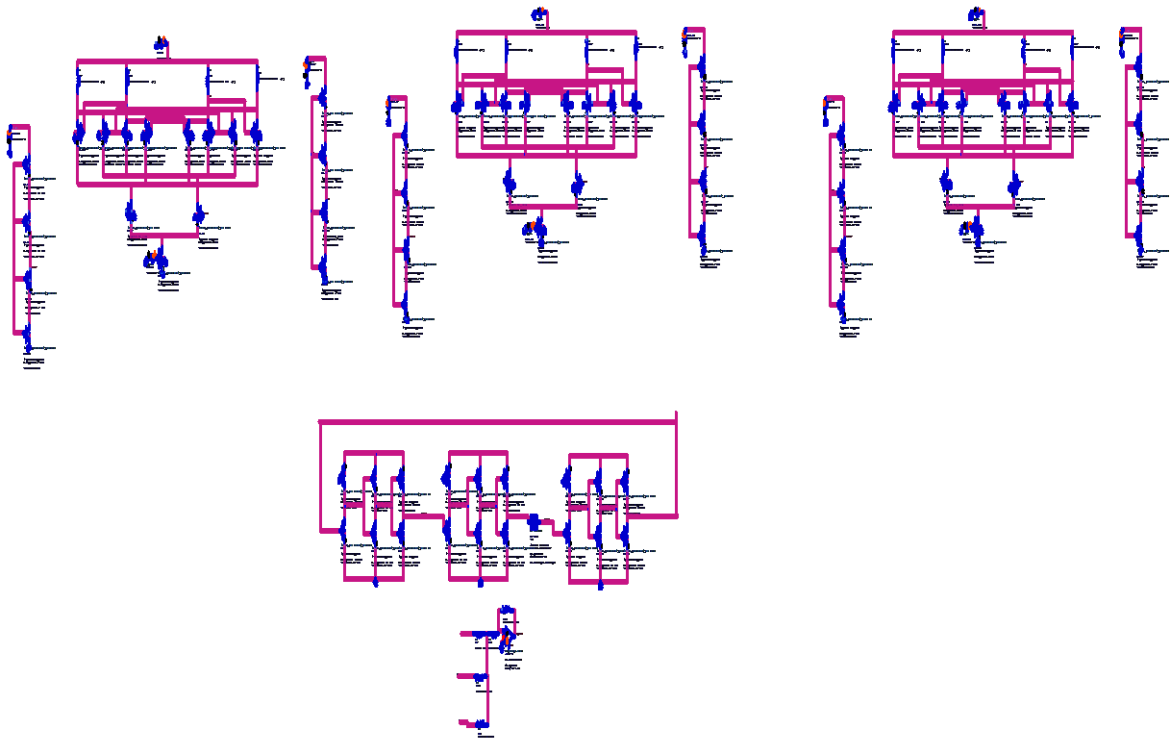

Figure 28: Ring oscillator with frequency divider and weighted summation circuit.

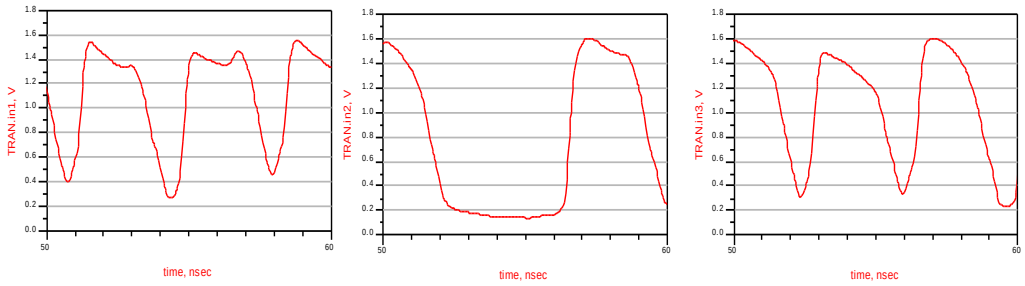

Figure 29: Generation of various frequencies using the ring oscillator by the help of programmable frequency divider.

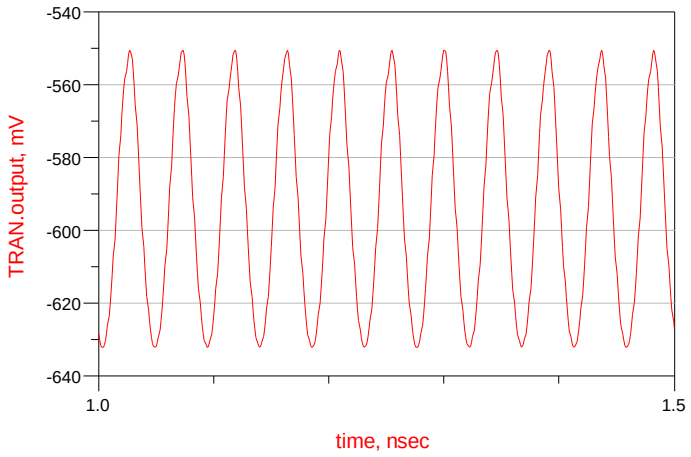

Figure 30: The output of the weighted summation of signals with various frequencies.

Conclusion

In this research, the dual-gate and ring oscillators were studied. The aim of the ring oscillator design with dual-gate transistor was that a sinusoidal signal with low distortion could be generated. In addition, we observed that compared to the MOSFET transistor, the dual-gate transistor had a higher frequency. In the next step, using the weighted summation method with various sinusoidal signals, different waveforms were generated. For this purpose, there was a need for an operational amplifier that this operational amplifier was designed and simulated. In addition, in order to generate various signals, we needed different frequencies that in this research, a frequency divider was also designed so it could generate various frequencies using the designed phase shift oscillator, and therefore, as a result, various signals using the weighted summation method could be generated. The performed design was simulated using HSPICE and ADS.

In the next step, a ring oscillator circuit was proposed and designed. Various signals were designed using the designed oscillator circuit and the frequency divider circuit. Finally, the three outputs were weighted summed together and it was shown that the oscillations with three times of frequency could be generated using the weighted summation of the phase shift oscillator output. Therefore, according to the results, the following proposals will be presented:

- Designing the ring oscillator with more stories.
- Generating triangular and square signals using the frequency divider and ring oscillator.
- Designing the complete differential ring oscillator circuit.

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